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MS-A6131 Ver: 2.0

CPU:

Celeron 1037,BGA- 1023pin

System Chipset:

Intel NM70

OnBoard Chipset:

HD Audio Codec:ALC887 CG

LAN:Realtek RTL8111G

SIO : NUVOTON NCT6104

CARD READER :Realtek RTS5249

Single Touch MER4485

USB3.0 : Asmedia1042AE

Main Memory:

DDRIII (1066/1333MHz) * 1

Expansion Slots:

MINIPCI Express (X1) Slot * 1

PWM:

Controller:ISL95837 1+1Phase CPU+GPU

Controller:TPS51211 CPU_VTT

Controller:TPS51216 VCC_DDR

Other:

VGA * 1

eDP * 1

USB2.0 * 4(colay with USB 3.0 * 2)

SATA 3.0 * 1(HDD)

SATA 2.0 * 1(ODD)

LPT Port * 1

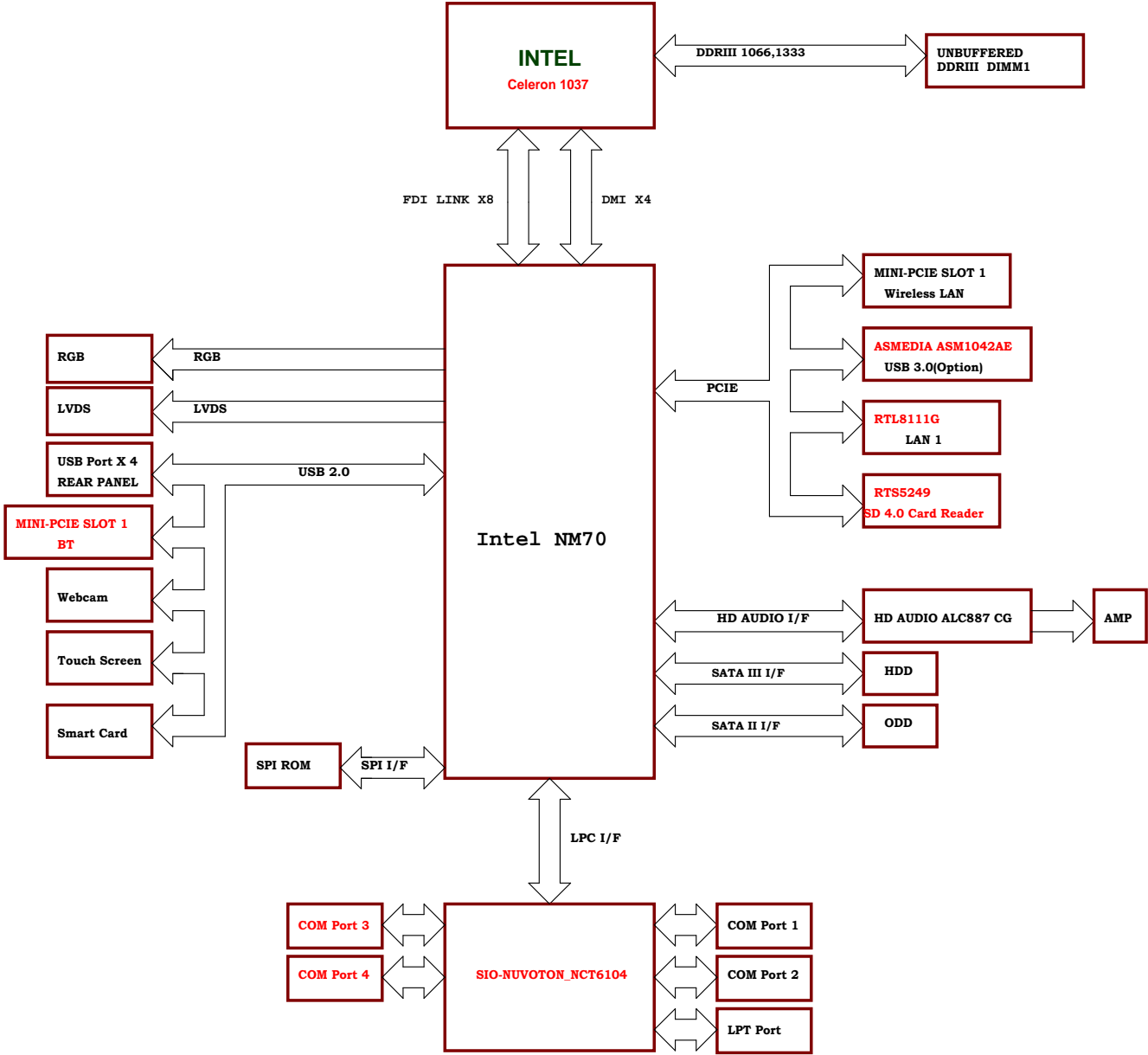
COM Port * 4

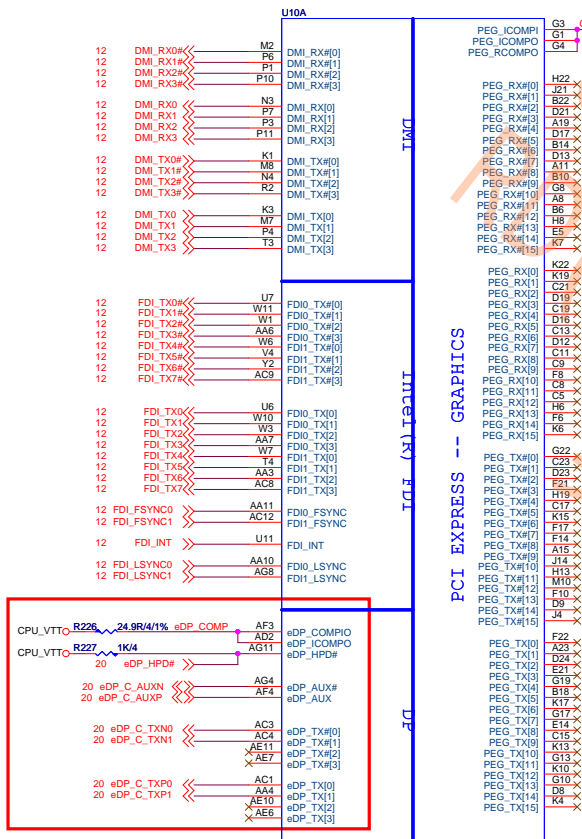
Card reader * 1(3 in 1)

Smart Card * 1

MS-A6131 Ver : 2.0

Block Diagram



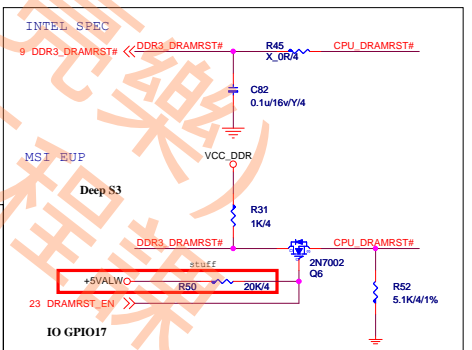
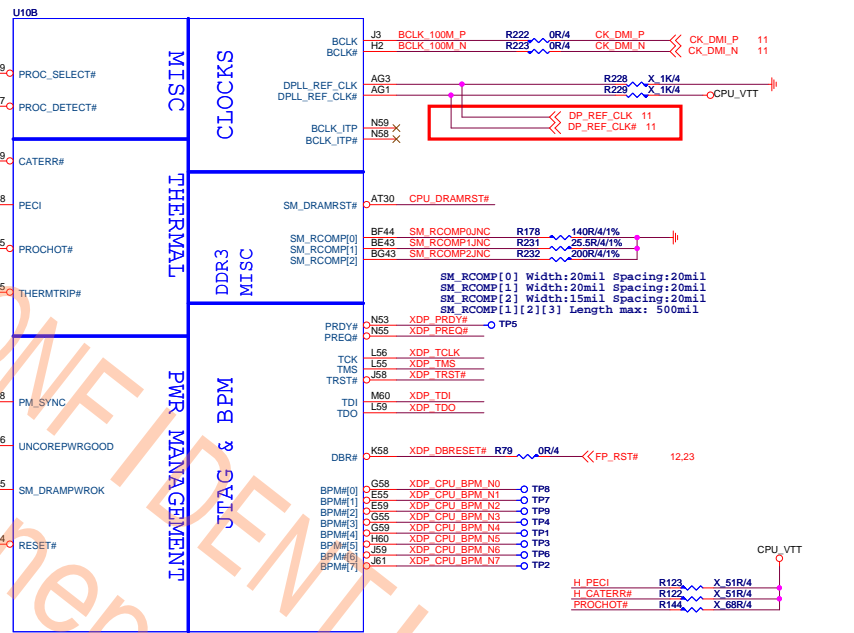
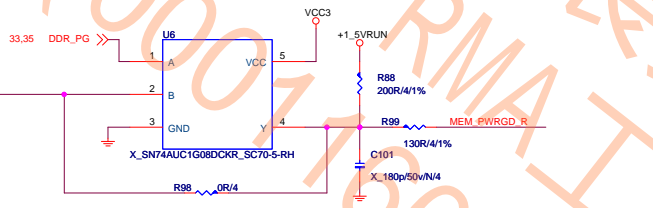
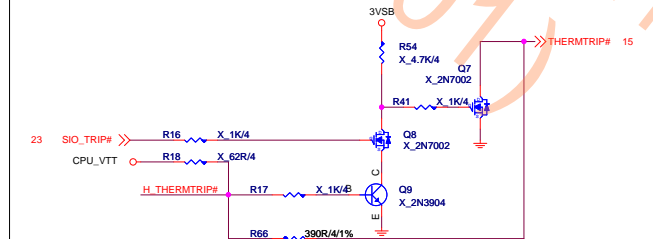
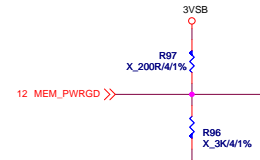
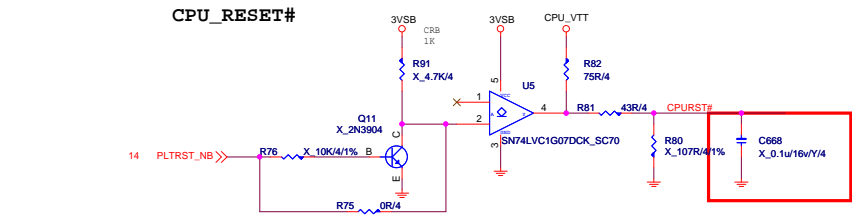


PCI EXPRESS -- GRAPHICS

DP

Intel Comments:
eDP COMP signals are required
if integrated gfx is enabled even
if eDP interface is disabled.

AV8062700852800_BGA1023-HF-1



9 MEM_MA_DATA[63..0] <<>

U10C

MEM_MA_DATA0 AG6 SA_DQ[0]
MEM_MA_DATA1 AJ6 SA_DQ[1]
MEM_MA_DATA2 AP11 SA_DQ[2]
MEM_MA_DATA3 AL6 SA_DQ[3]
MEM_MA_DATA4 AJ10 SA_DQ[4]
MEM_MA_DATA5 AJ8 SA_DQ[5]
MEM_MA_DATA6 AL8 SA_DQ[6]
MEM_MA_DATA7 AL7 SA_DQ[7]
MEM_MA_DATA8 AR11 SA_DQ[8]
MEM_MA_DATA9 AP6 SA_DQ[9]
MEM_MA_DATA10 AU6 SA_DQ[10]
MEM_MA_DATA11 AV9 SA_DQ[11]
MEM_MA_DATA12 AR6 SA_DQ[12]
MEM_MA_DATA13 AP8 SA_DQ[13]
MEM_MA_DATA14 AT13 SA_DQ[14]
MEM_MA_DATA15 AU13 SA_DQ[15]
MEM_MA_DATA16 BC7 SA_DQ[16]
MEM_MA_DATA17 BB7 SA_DQ[17]
MEM_MA_DATA18 BA13 SA_DQ[18]
MEM_MA_DATA19 BB11 SA_DQ[19]
MEM_MA_DATA20 BA7 SA_DQ[20]
MEM_MA_DATA21 BA9 SA_DQ[21]
MEM_MA_DATA22 BB9 SA_DQ[22]
MEM_MA_DATA23 AY13 SA_DQ[23]
MEM_MA_DATA24 AV14 SA_DQ[24]
MEM_MA_DATA25 AR14 SA_DQ[25]
MEM_MA_DATA26 AR17 SA_DQ[26]
MEM_MA_DATA27 AR19 SA_DQ[27]
MEM_MA_DATA28 BA14 SA_DQ[28]
MEM_MA_DATA29 AU14 SA_DQ[29]
MEM_MA_DATA30 BB14 SA_DQ[30]
MEM_MA_DATA31 BB17 SA_DQ[31]
MEM_MA_DATA32 BA45 SA_DQ[32]
MEM_MA_DATA33 AR43 SA_DQ[33]
MEM_MA_DATA34 AW48 SA_DQ[34]
MEM_MA_DATA35 BC48 SA_DQ[35]
MEM_MA_DATA36 BC45 SA_DQ[36]
MEM_MA_DATA37 AR45 SA_DQ[37]
MEM_MA_DATA38 AT48 SA_DQ[38]
MEM_MA_DATA39 AY48 SA_DQ[39]
MEM_MA_DATA40 BA49 SA_DQ[40]
MEM_MA_DATA41 AV49 SA_DQ[41]
MEM_MA_DATA42 BB51 SA_DQ[42]
MEM_MA_DATA43 AY63 SA_DQ[43]
MEM_MA_DATA44 BB49 SA_DQ[44]
MEM_MA_DATA45 AU49 SA_DQ[45]
MEM_MA_DATA46 BA53 SA_DQ[46]
MEM_MA_DATA47 BB55 SA_DQ[47]
MEM_MA_DATA48 BA55 SA_DQ[48]
MEM_MA_DATA49 AV56 SA_DQ[49]
MEM_MA_DATA50 AP50 SA_DQ[50]
MEM_MA_DATA51 AP53 SA_DQ[51]
MEM_MA_DATA52 AV54 SA_DQ[52]
MEM_MA_DATA53 AT54 SA_DQ[53]
MEM_MA_DATA54 AP56 SA_DQ[54]
MEM_MA_DATA55 AP52 SA_DQ[55]
MEM_MA_DATA56 AN57 SA_DQ[56]
MEM_MA_DATA57 AN53 SA_DQ[57]
MEM_MA_DATA58 AG56 SA_DQ[58]
MEM_MA_DATA59 AG53 SA_DQ[59]
MEM_MA_DATA60 AN55 SA_DQ[60]
MEM_MA_DATA61 AN52 SA_DQ[61]
MEM_MA_DATA62 AG55 SA_DQ[62]
MEM_MA_DATA63 AK56 SA_DQ[63]

DDR SYSTEM MEMORY A

SA_CK[0]
SA_CK#0
SA_CKE[0]

SA_CK[1]
SA_CK#1
SA_CKE[1]

SA_CS#0
SA_CS#1

SA_ODT[0]
SA_ODT[1]

SA_DQS#0
SA_DQS#1
SA_DQS#2
SA_DQS#3
SA_DQS#4
SA_DQS#5
SA_DQS#6
SA_DQS#7

SA_DQS[0]
SA_DQS[1]
SA_DQS[2]
SA_DQS[3]
SA_DQS[4]
SA_DQS[5]
SA_DQS[6]
SA_DQS[7]

SA_MA[0]
SA_MA[1]
SA_MA[2]
SA_MA[3]
SA_MA[4]
SA_MA[5]
SA_MA[6]
SA_MA[7]
SA_MA[8]
SA_MA[9]
SA_MA[10]
SA_MA[11]
SA_MA[12]
SA_MA[13]
SA_MA[14]
SA_MA[15]

AU36 MEM_MA_CLK_H0 MEM_MA_CLK_H0 9
AV36 MEM_MA_CLK_L0 MEM_MA_CLK_L0 9
AY26 MEM_MA_CKE0 MEM_MA_CKE0 9

AT40 MEM_MA_CLK_H1 MEM_MA_CLK_H1 9
AU40 MEM_MA_CLK_L1 MEM_MA_CLK_L1 9
BB26 MEM_MA_CKE1 MEM_MA_CKE1 9

BB40 MEM_MA_CS_L0 MEM_MA_CS_L0 9
BC41 MEM_MA_CS_L1 MEM_MA_CS_L1 9

AY40 MEM_MA_ODT0 MEM_MA_ODT0 9
BA41 MEM_MA_ODT1 MEM_MA_ODT1 9

AL11 MEM_MA_DQS_L0 MEM_MA_DQS_L0 9
AR8 MEM_MA_DQS_L1 MEM_MA_DQS_L1 9
AY11 MEM_MA_DQS_L2 MEM_MA_DQS_L2 9
AT17 MEM_MA_DQS_L3 MEM_MA_DQS_L3 9
AV45 MEM_MA_DQS_L4 MEM_MA_DQS_L4 9
AY51 MEM_MA_DQS_L5 MEM_MA_DQS_L5 9
AT55 MEM_MA_DQS_L6 MEM_MA_DQS_L6 9
AK55 MEM_MA_DQS_L7 MEM_MA_DQS_L7 9

AJ11 MEM_MA_DQS_H0 MEM_MA_DQS_H0 9
AR10 MEM_MA_DQS_H1 MEM_MA_DQS_H1 9
AY11 MEM_MA_DQS_H2 MEM_MA_DQS_H2 9
AU17 MEM_MA_DQS_H3 MEM_MA_DQS_H3 9
AV45 MEM_MA_DQS_H4 MEM_MA_DQS_H4 9
AU58 MEM_MA_DQS_H5 MEM_MA_DQS_H5 9
AT56 MEM_MA_DQS_H6 MEM_MA_DQS_H6 9
AK54 MEM_MA_DQS_H7 MEM_MA_DQS_H7 9

BG35 MEM_MA_ADD0 MEM_MA_ADD[15..0] 9
BB34 MEM_MA_ADD1
BE35 MEM_MA_ADD2
BD35 MEM_MA_ADD3

AT34 MEM_MA_ADD4
AU34 MEM_MA_ADD5
BB32 MEM_MA_ADD6
AT32 MEM_MA_ADD7
AY32 MEM_MA_ADD8
AV32 MEM_MA_ADD9
BE37 MEM_MA_ADD10
BA30 MEM_MA_ADD11
BC30 MEM_MA_ADD12
AW41 MEM_MA_ADD13
AY28 MEM_MA_ADD14
AU26 MEM_MA_ADD15

U10D

AL4 SB_DQ[0]
AL1 SB_DQ[1]
AN3 SB_DQ[2]
AR4 SB_DQ[3]
AK3 SB_DQ[4]
AN4 SB_DQ[5]
SA SB_DQ[6]
AR1 SB_DQ[7]
AU4 SB_DQ[8]
AY2 SB_DQ[9]
AV4 SB_DQ[10]
BA4 SB_DQ[11]
AU3 SB_DQ[12]
AR3 SB_DQ[13]
BA3 SB_DQ[14]
BE9 SB_DQ[15]
BD9 SB_DQ[16]
BD13 SB_DQ[17]
BF12 SB_DQ[18]
BF8 SB_DQ[19]
BD10 SB_DQ[20]
BD14 SB_DQ[21]
BE13 SB_DQ[22]
BF16 SB_DQ[23]
BE17 SB_DQ[24]
BE18 SB_DQ[25]
BE21 SB_DQ[26]
BE14 SB_DQ[27]
BG14 SB_DQ[28]
BG18 SB_DQ[29]
AR8 SB_DQ[30]
BD50 SB_DQ[31]
BF48 SB_DQ[32]
BD53 SB_DQ[33]
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BD54 SB_DQ[38]
BE53 SB_DQ[39]
BF56 SB_DQ[40]
BE57 SB_DQ[41]
BC58 SB_DQ[42]
AY60 SB_DQ[43]
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AK58 SB_DQ[56]
AL58 SB_DQ[57]
AG59 SB_DQ[58]
AL58 SB_DQ[59]
AL59 SB_DQ[60]
AF61 SB_DQ[61]
AH60 SB_DQ[62]
SB_DQ[63]

DDR SYSTEM MEMORY B

SB_CK[0]
SB_CK#0
SB_CKE[0]

SB_CK[1]
SB_CK#1
SB_CKE[1]

SB_CS#0
SB_CS#1

SB_ODT[0]
SB_ODT[1]

SB_DQS#0
SB_DQS#1
SB_DQS#2
SB_DQS#3
SB_DQS#4
SB_DQS#5
SB_DQS#6
SB_DQS#7

SB_DQS[0]
SB_DQS[1]
SB_DQS[2]
SB_DQS[3]
SB_DQS[4]
SB_DQS[5]
SB_DQS[6]
SB_DQS[7]

SB_MA[0]
SB_MA[1]
SB_MA[2]
SB_MA[3]
SB_MA[4]
SB_MA[5]
SB_MA[6]
SB_MA[7]
SB_MA[8]
SB_MA[9]
SB_MA[10]
SB_MA[11]
SB_MA[12]
SB_MA[13]
SB_MA[14]
SB_MA[15]

BA34
AY34
AR22

BA36
BB36
BF27

BE41
BE47

AT43
BG47

AL3
AV3
BG11
BD17
BG5
BA59
AT60
AK59

AM2
AV1
BE11
BD18
BE51
BA61
AR59
AK61

BF32
BE33
BD33
AU30
BD30
AV30
BG30
BD29
BE30
BE28
BD43
AT28
AV28
BD46
AT26
AU22

BG39 SB_BS[0]
BD42 SB_BS[1]
AT22 SB_BS[2]

AV43 SB_CAS#
BF40 SB_RAS#
BD45 SB_WE#

AV8062700852800_BGA1023-HF-1

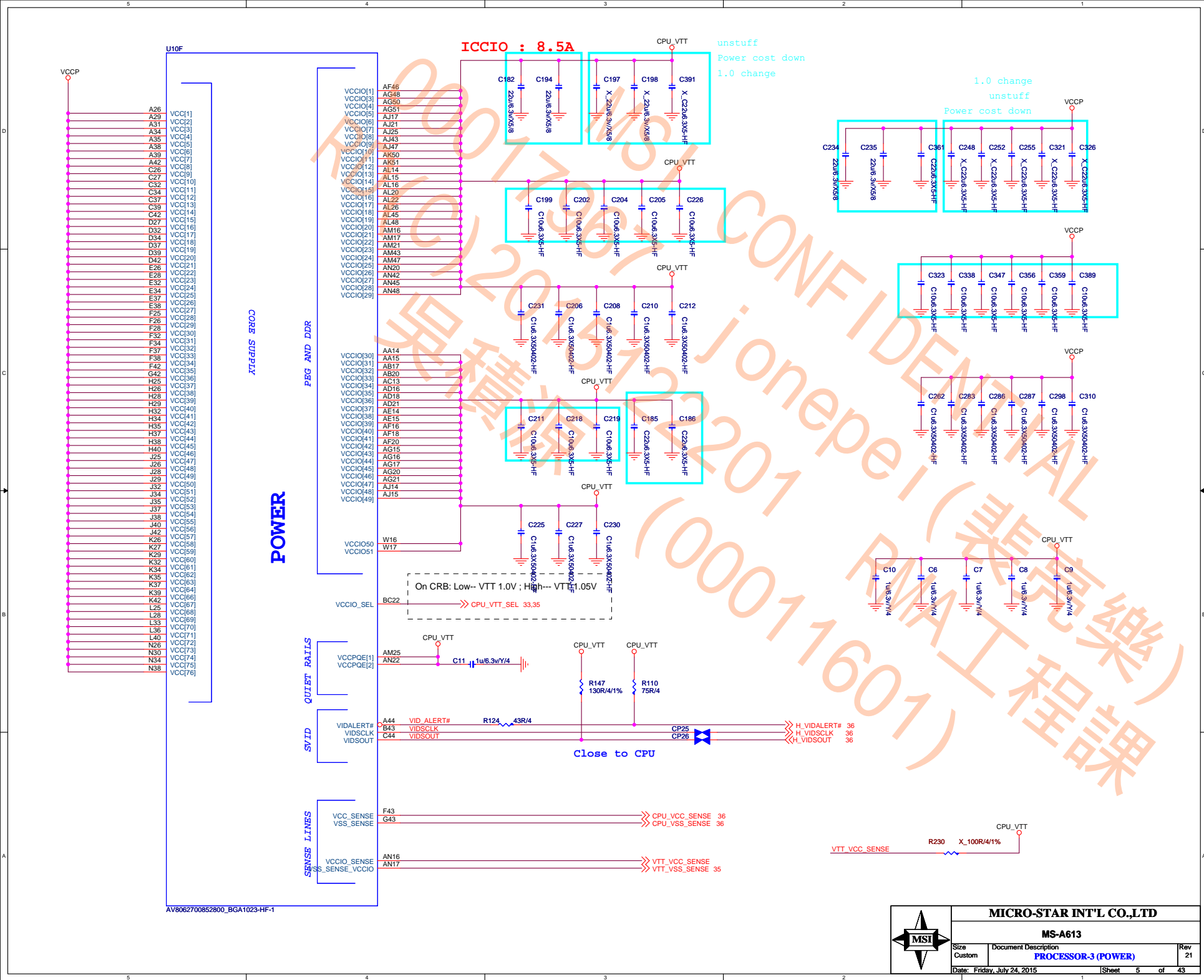
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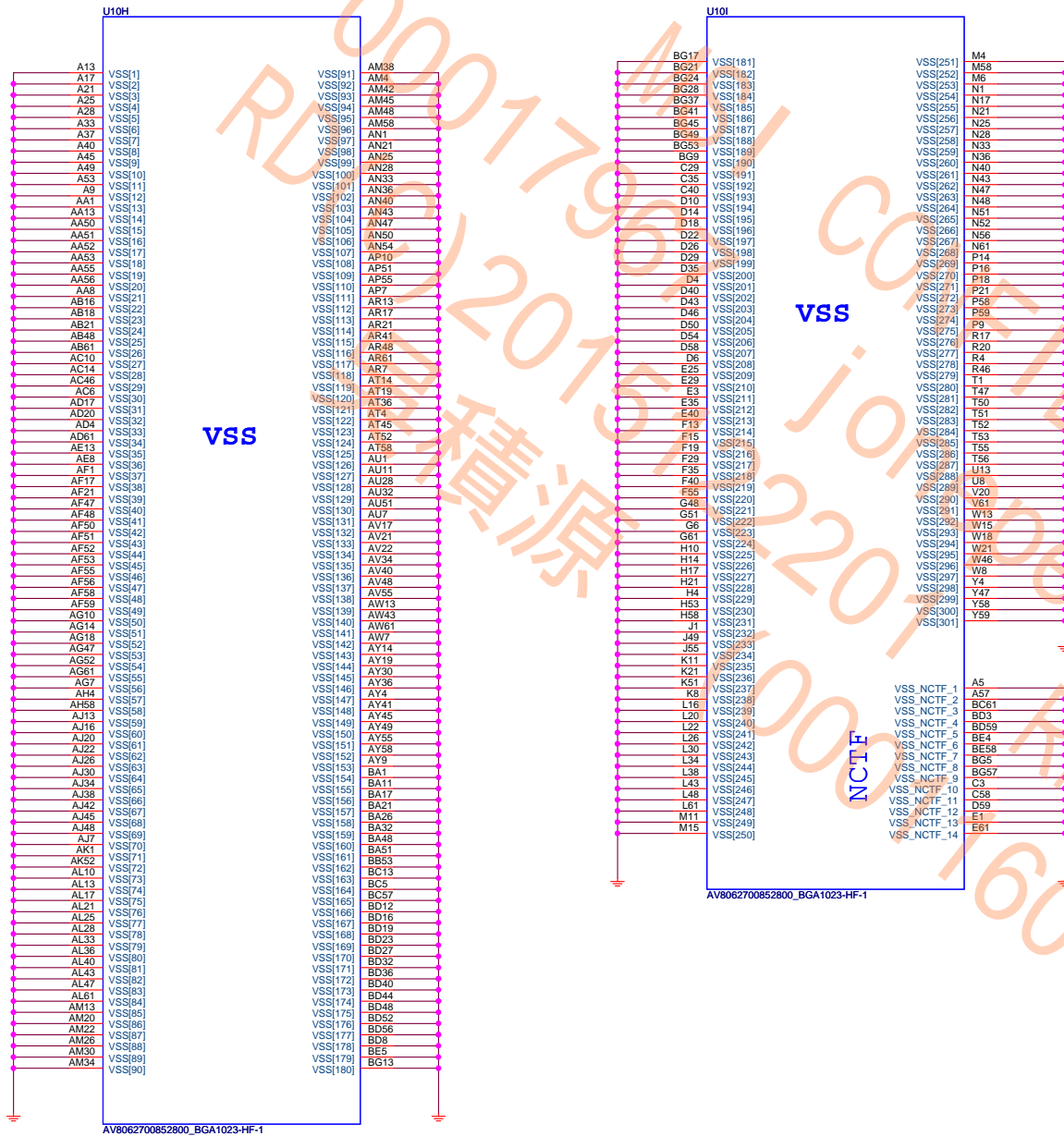


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MS-A613

Size	Document Description	Rev
Custom	PROCESSOR-2 (DDR3)	21
Date: Friday, July 24, 2015		Sheet 4 of 43





AV8062700852800_BGA1023-HF-1

AV8062700852800_BGA1023-HF-1

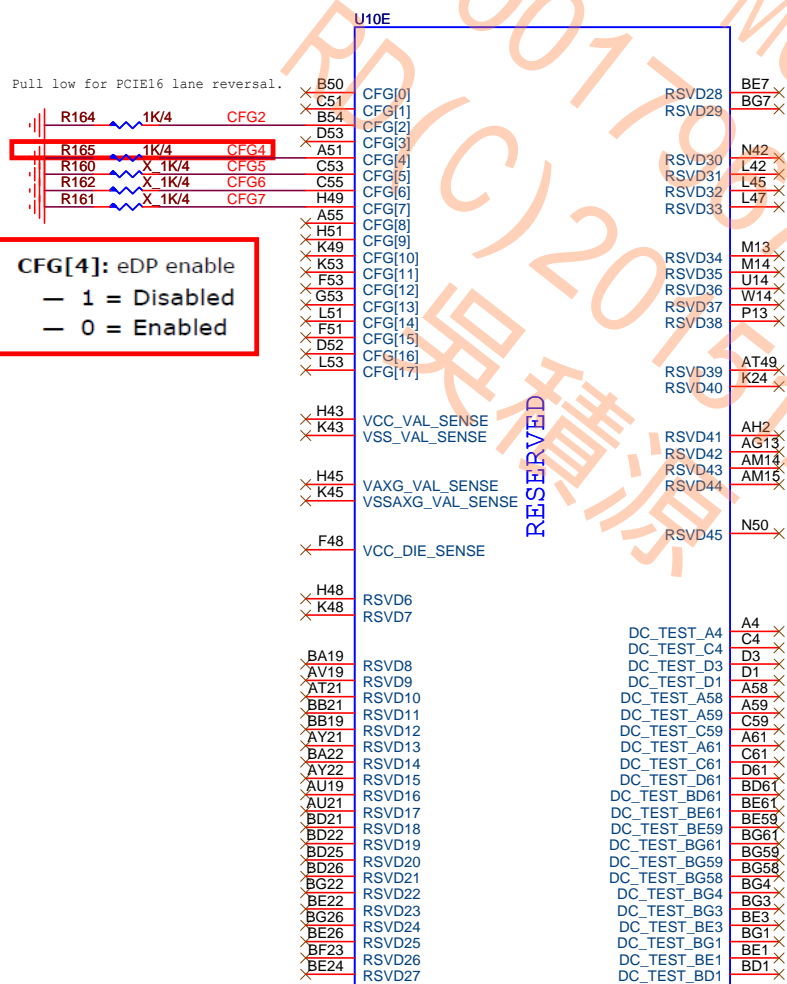


MICRO-STAR INT'L CO.,LTD

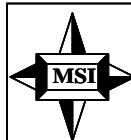
MS-A613

Size	Document Description	Rev
Custom	PROCESSOR-5 (GND)	21
Date: Friday, July 24, 2015		
Sheet 7 of 43		

SANDYBRIDGE PROCESSOR (RESERVED)



AV8062700852800_BGA1023-HF-1



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MS-A613

Size Custom

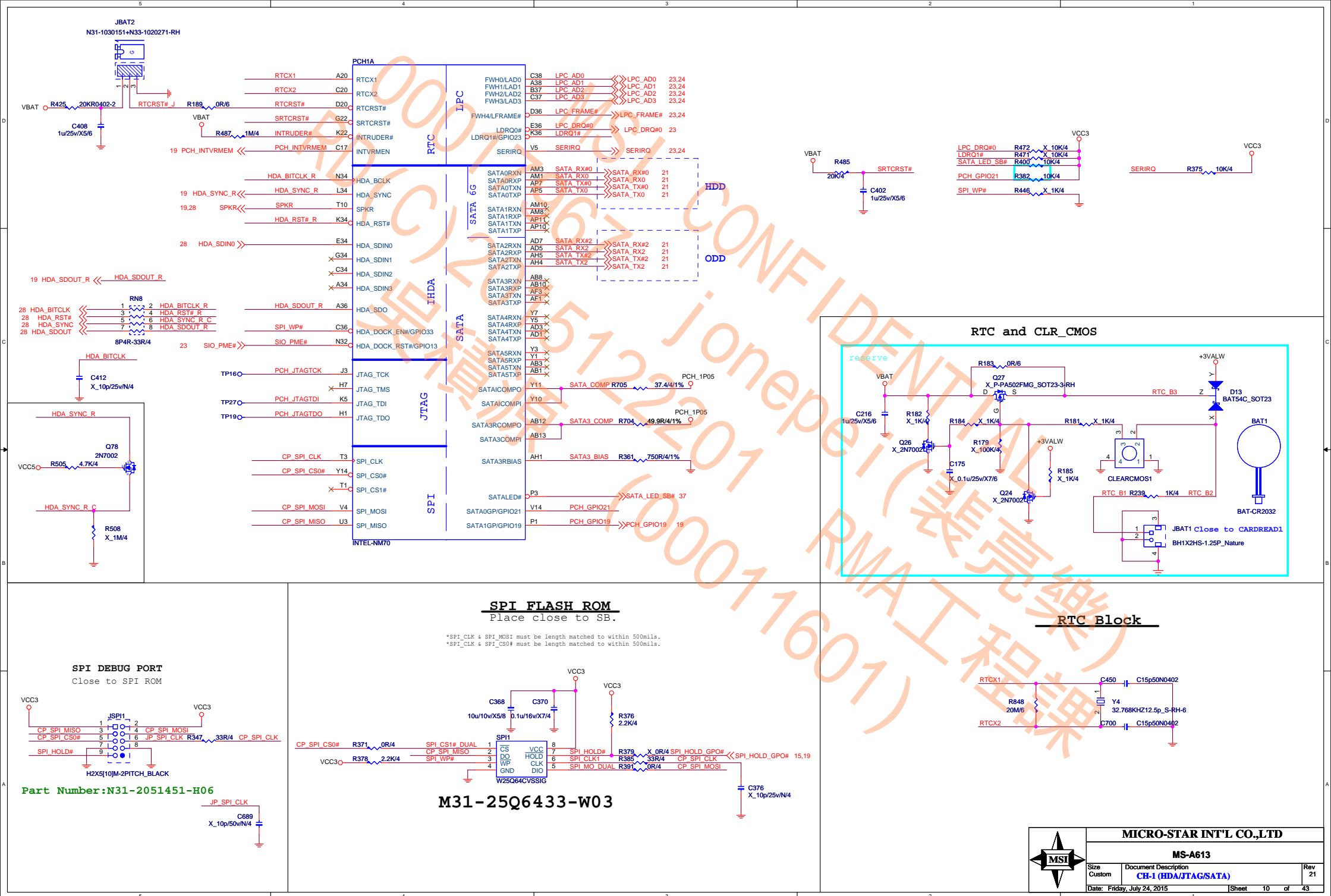
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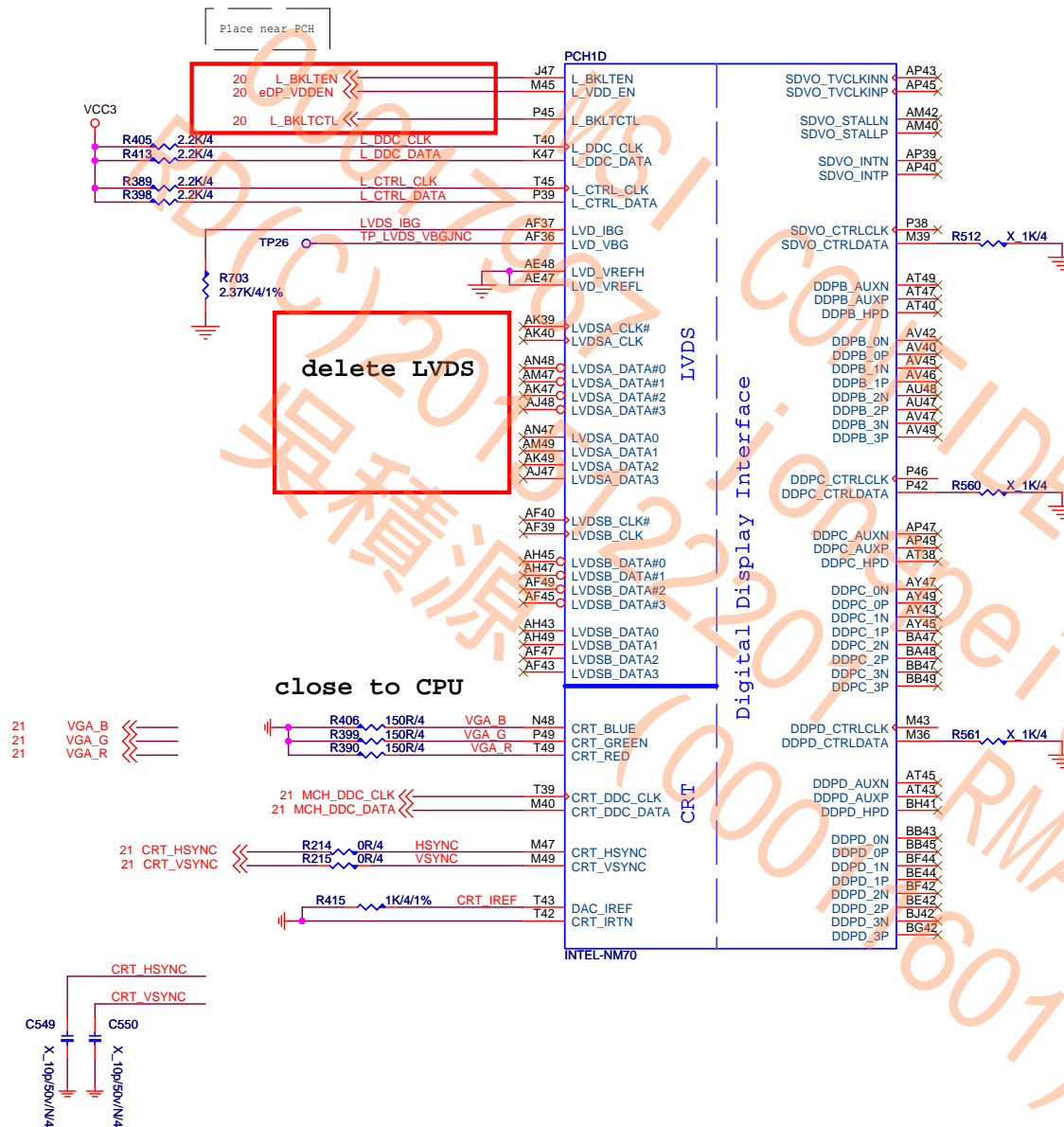
PROCESSOR-6 (RESERVE)

Rev 21

Date: Friday, July 24, 2015

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MS-A613

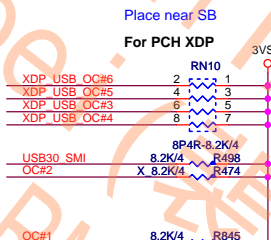
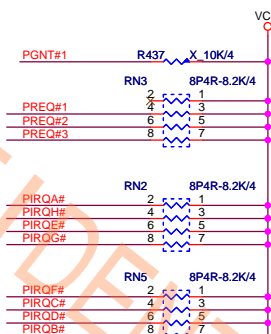
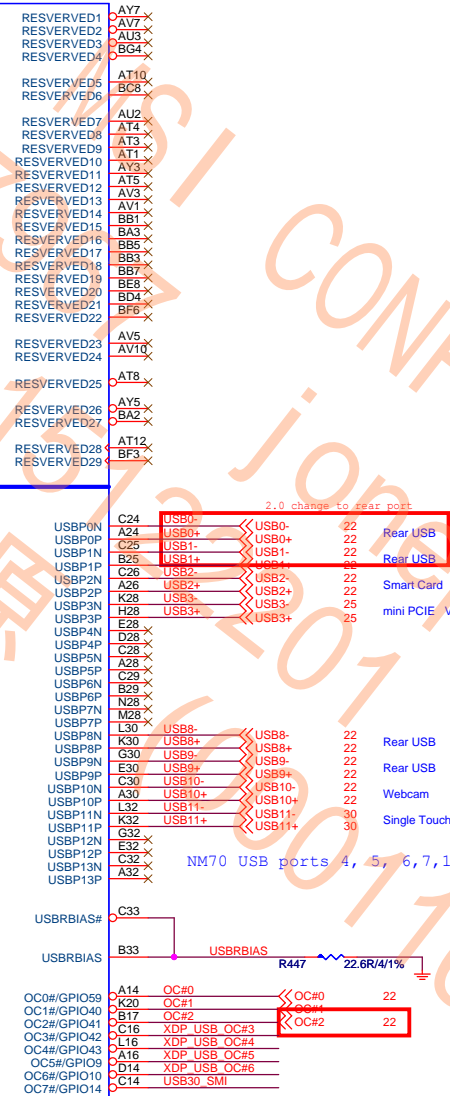
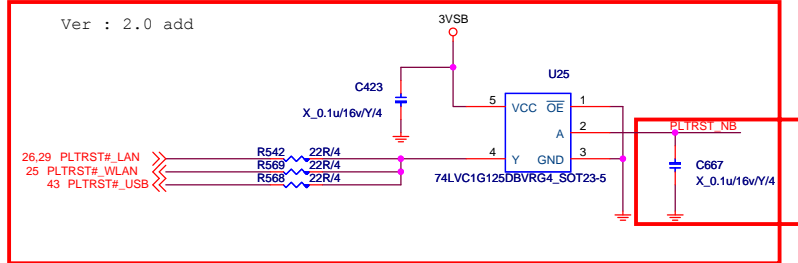
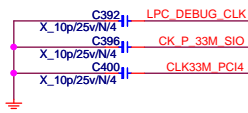
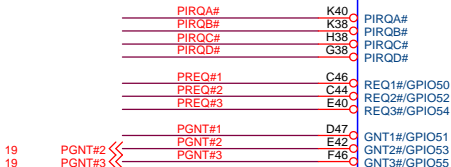
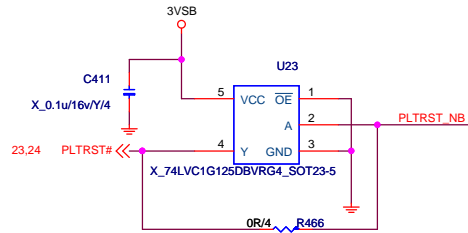
Size
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Document Description
PCH-4 (LVDS/DDI/VGA)

Rev
21

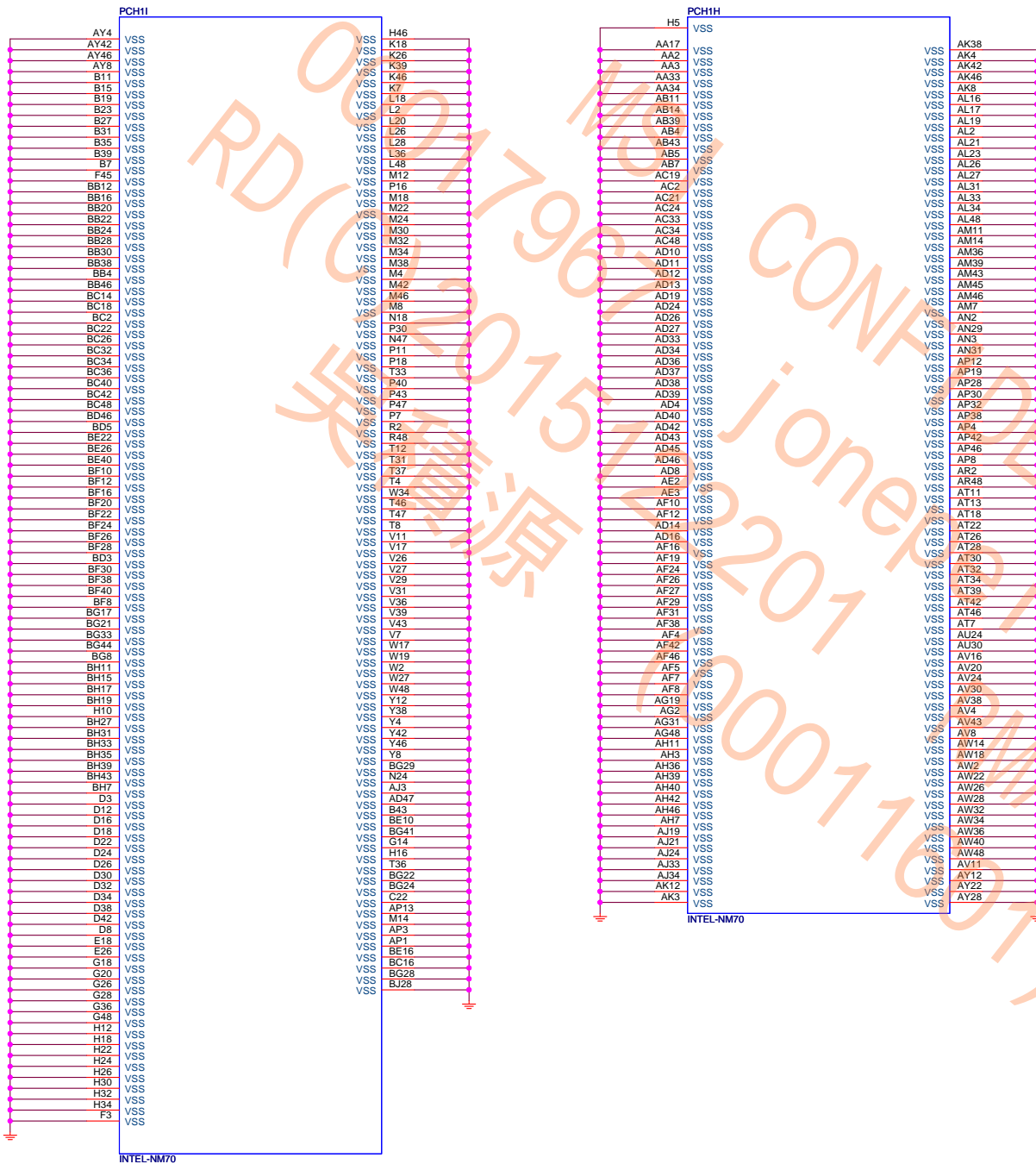
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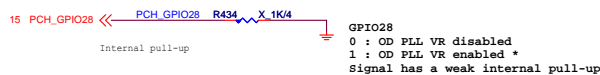
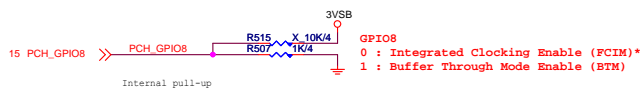
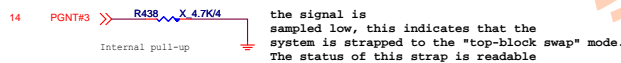
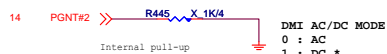
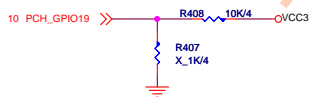
NM70 USB ports 4, 5, 6, 7, 12 and 13 are disabled



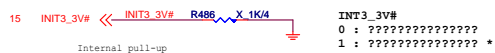


CP REQUIRED STRAPS

BOOT DEVICE	GNT1	SATA1P/GPIO19
LPC	0	0
Reserved	0	1
PCI	1	0
SPI	1	1



PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

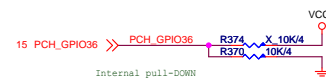


1. This signal should not be pulled low.
2. The internal pull-up is disabled after PLTRST# deasserts.

DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same voltage (DC coupling mode)default

GPIO36 --CRB connector to 3V

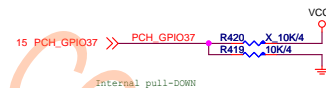
FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same voltage (DC coupling mode)default



Cougar point EDS PAGE:93 This signal should not be pull high

PCH EDS1.0:GP1036&37 should not be pulled high when strap is sampled.
PCH EDS1.1:GP1036&37 when pins are unused as SATAGP or GPIO, terminate them to VSS via 8.2k-10k resistor.

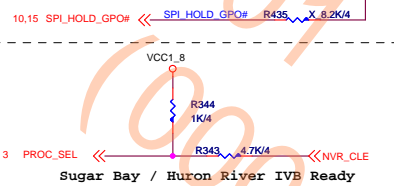
Cougar point EDS PAGE:93 This signal should not be pull high



HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



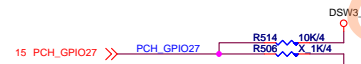
GPI015
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY

DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

INTVRMEM
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *



When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

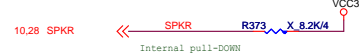


In Deep Sleep Power Well.
If not used,require a weak pull-up(8.2k-10k) to VccDSW3_3

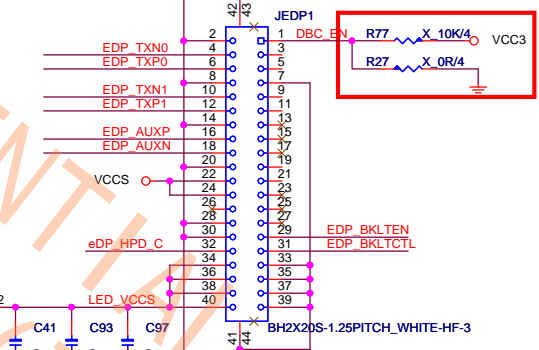
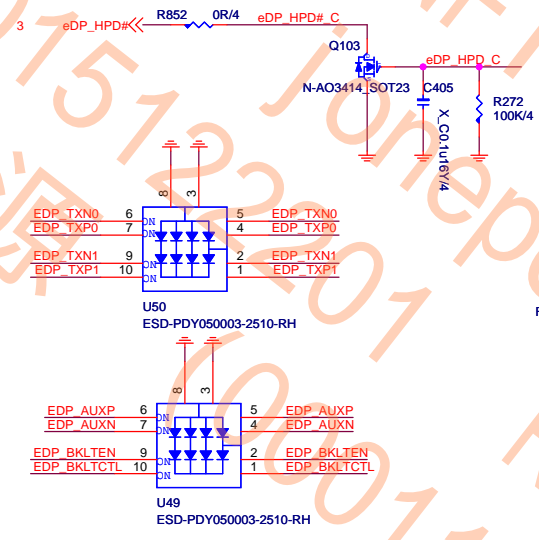
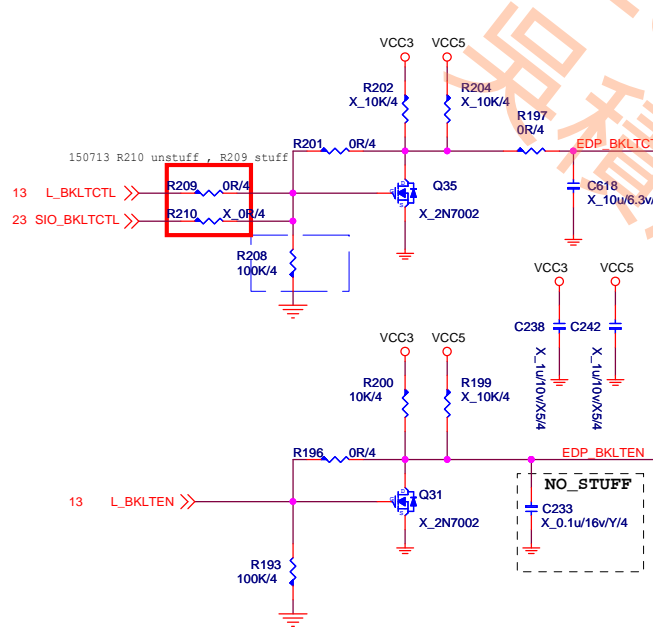
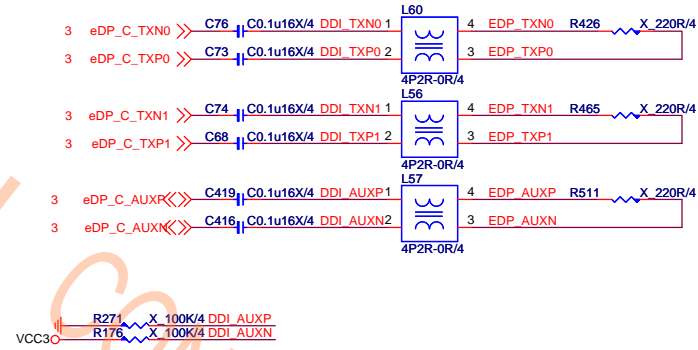
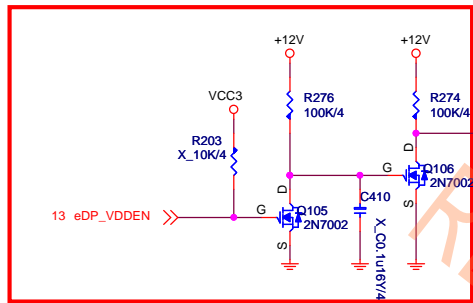


DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

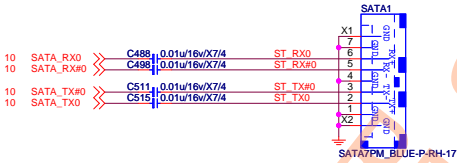


SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

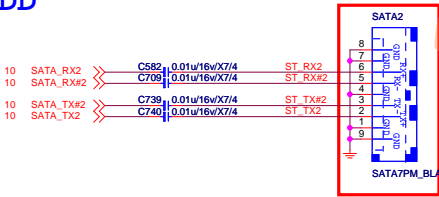


MICRO-STAR INT'L CO.,LTD			
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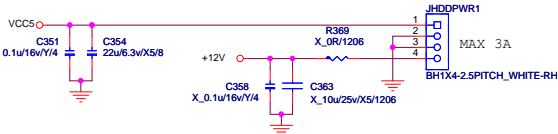
SATA HDD 2.5" N5N-07M2101-H06 (SATA3,Blue)



SATA ODD

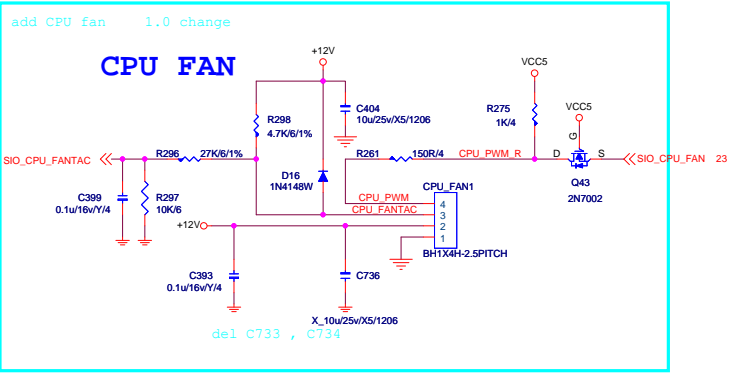


HDD Power



N32-1040D31-H06

更改為N32-1040D31-H06，增加定位柱



Cougar Point Platform Controller Hub
External Design Specification (EDS)

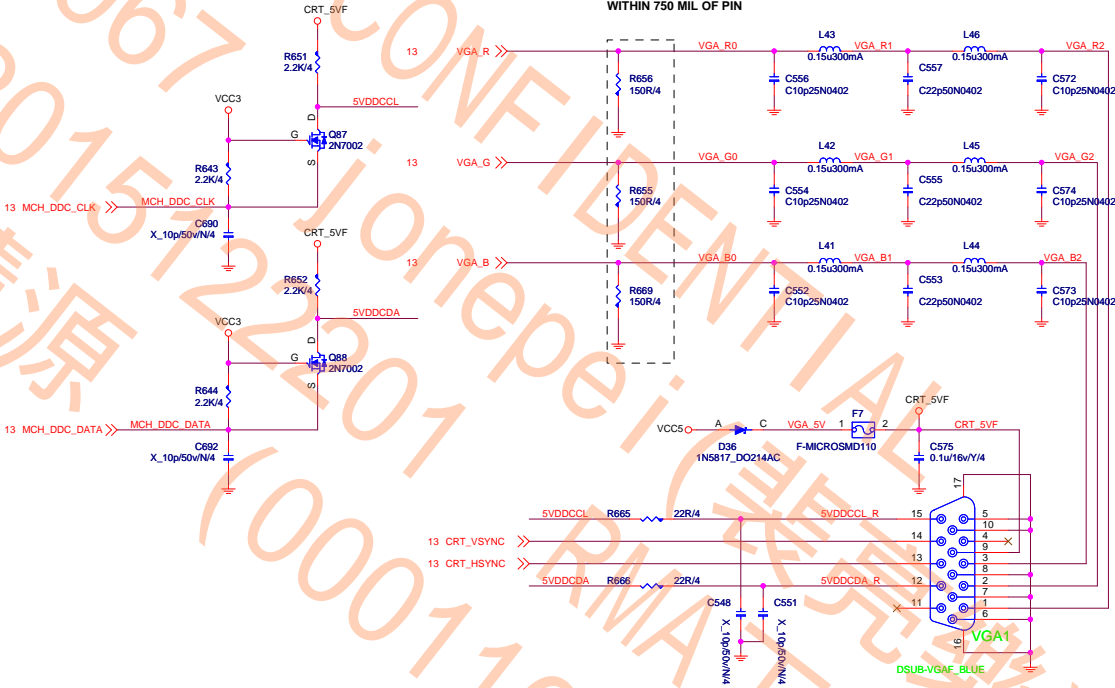
PCH Display Interfaces

The PCH's analog port uses an integrated 350 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 75 Hz.

Each Digital port is capable of driving a digital display up to 2560x1600 @ 60 Hz using DP and 1920x 1200 @ 60 Hz using HDMI, DVI (with reduced blanking).
LVDS 15.6" 1366 x 768 pixels resolution.

VGA (D-Sub) Connector

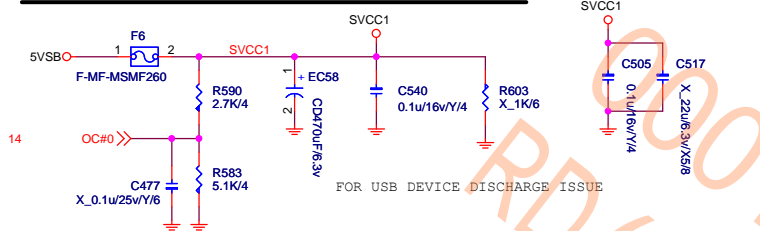
PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



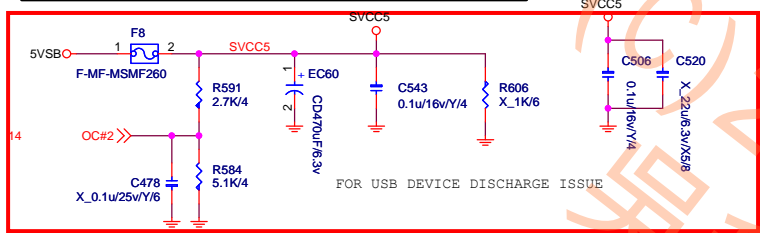
N51-15F0381-F02
Right Angle

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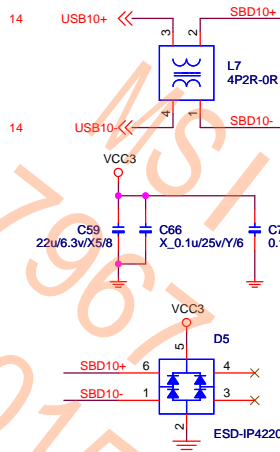
POWER CIRCUIT FOR USB PORT 8,9 (REAR)



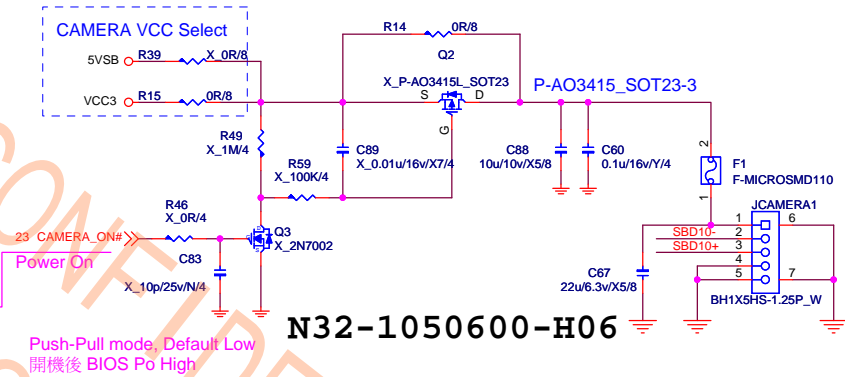
POWER CIRCUIT FOR USB PORT 0,1 (REAR)



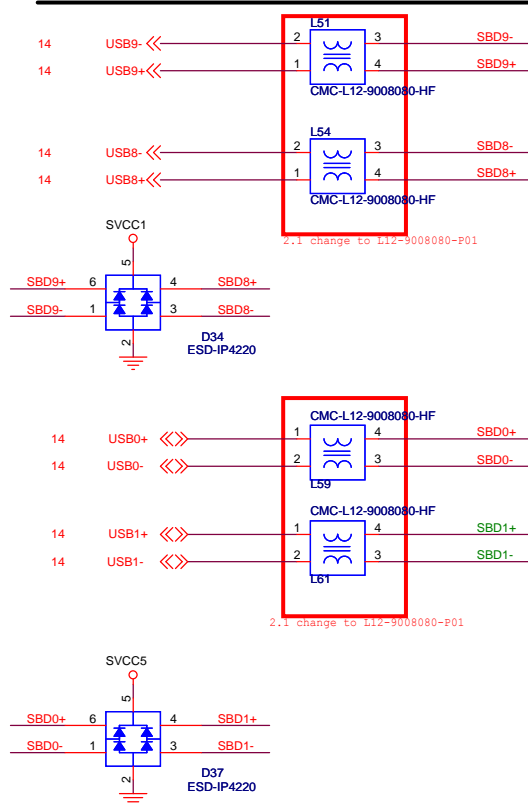
Webcam



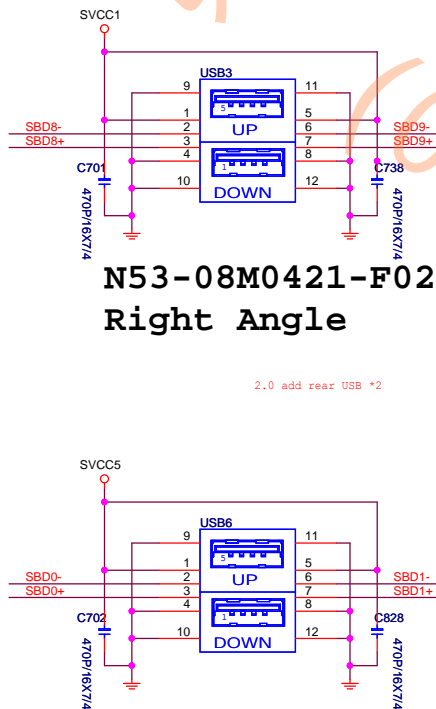
AOC & Channel VCC3 ViewSonic VCC5 (USB_STR2)



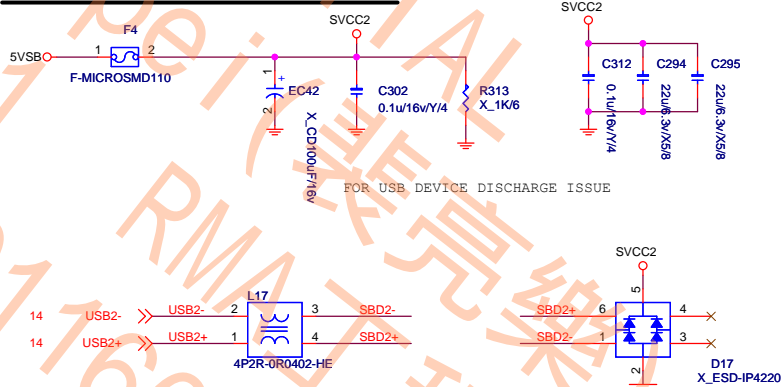
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



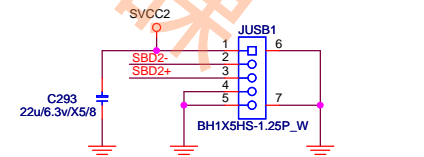
N53-08M0421-F02 Right Angle



POWER CIRCUIT FOR USB PORT 9



for Smart Card



N32-1050600-H06

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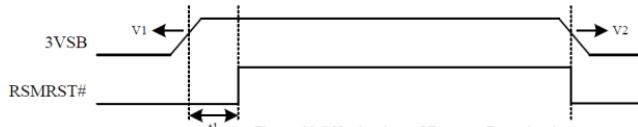
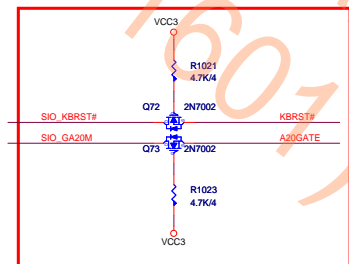
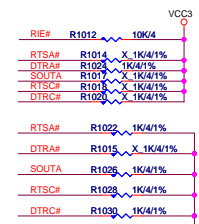
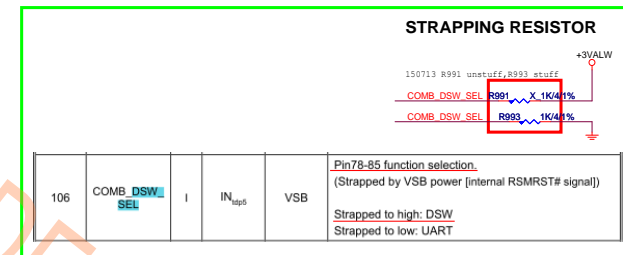
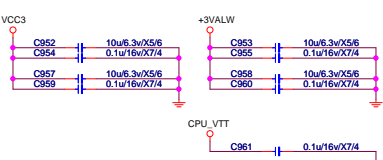
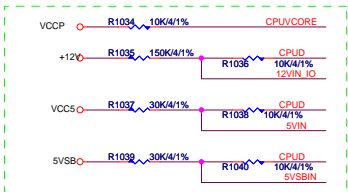
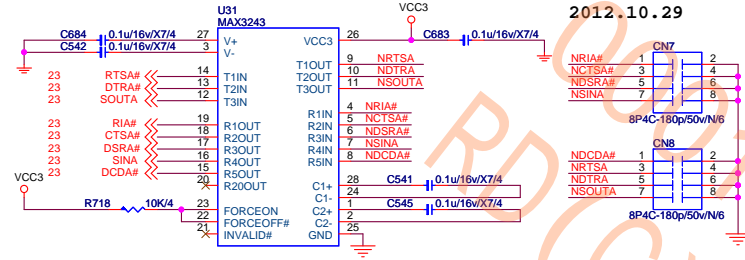


Table 16-3 Timing and Voltage Parameters of RSMRST#

POWER ON SETTING PIN						
PIN	Name	FUNCTION	0	1	Power	
106	COMB_DSW_SEL	COMB_DSW_SEL	UART	DSW		3VSB
51	RTS1#	2E_4E_SEL	2E	4E		3VCC
52	DTR1#	24_48_SEL	24M Clock Source	48M Clock Source		3VCC
54	SOUT1#	GPIO_PORT80_SEL	GPIO to PORT80 Disable	GPIO to PORT80 Enable		3VCC
111	RTS3#	SOUTC_P80_SEL	SOUTC to S0port disable	SOUTC to S0port enable		3VCC
112	DTR3#	SOUTE_P80_SEL	SOUTE to S0port disable	SOUTE to S0port enable		3VCC

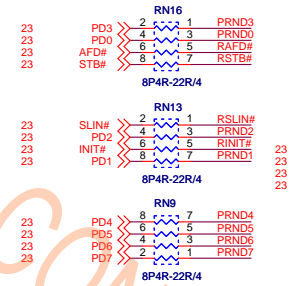


COM PORT 1

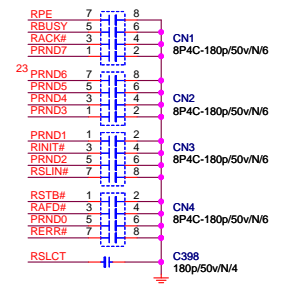


N51-09M0091-F02 change N51-09M0211-F02
2012.10.29

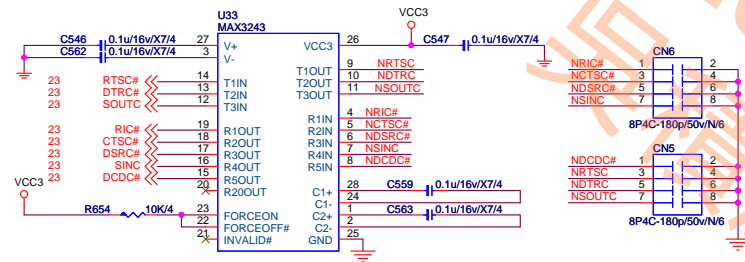
PARALLAL PORT



N31-2131281-H06
Vertical
Pitch 2.0 Pin Header

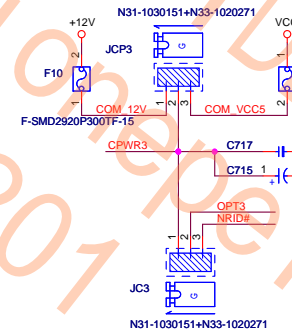
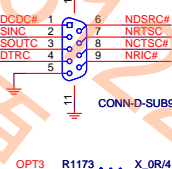


COM PORT 2



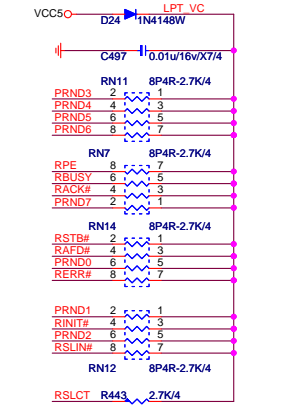
N51-09M0091-F02 change N51-09M0211-F02
2012.10.29

COM2

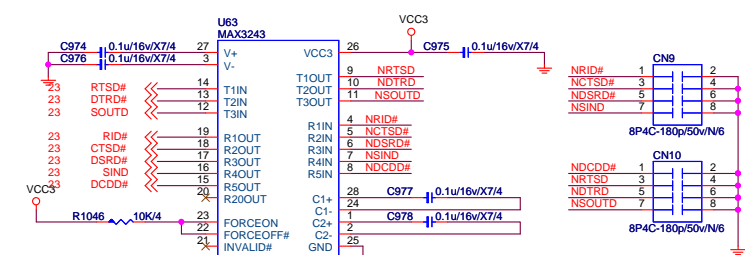


COM3 Function Select

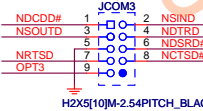
JCP3	1-2	2-3
Fun	12V	5V
JC3	1-2	2-3
Fun	PWR	RIN



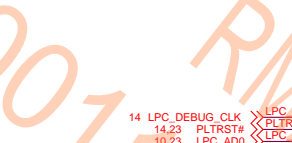
COM PORT 3



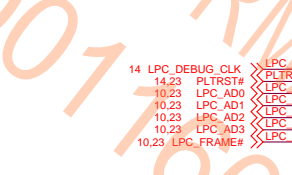
COM PORT 3



N31-2051331-H06



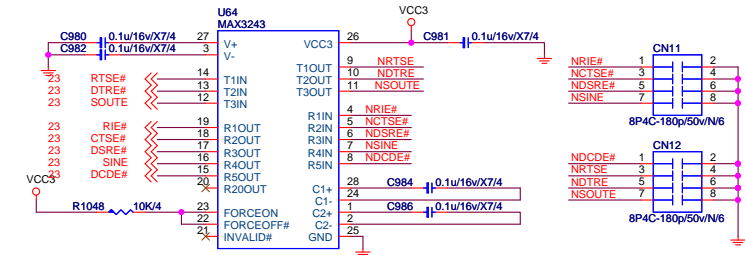
TPM / Port 80 HEADER



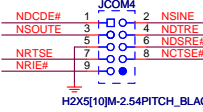
N31-2071201-H06
Right Angle



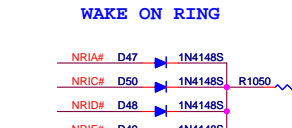
COM PORT 4



COM PORT 4



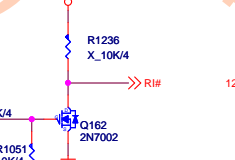
N31-2051331-H06



WAKE ON RING



WAKE ON RING

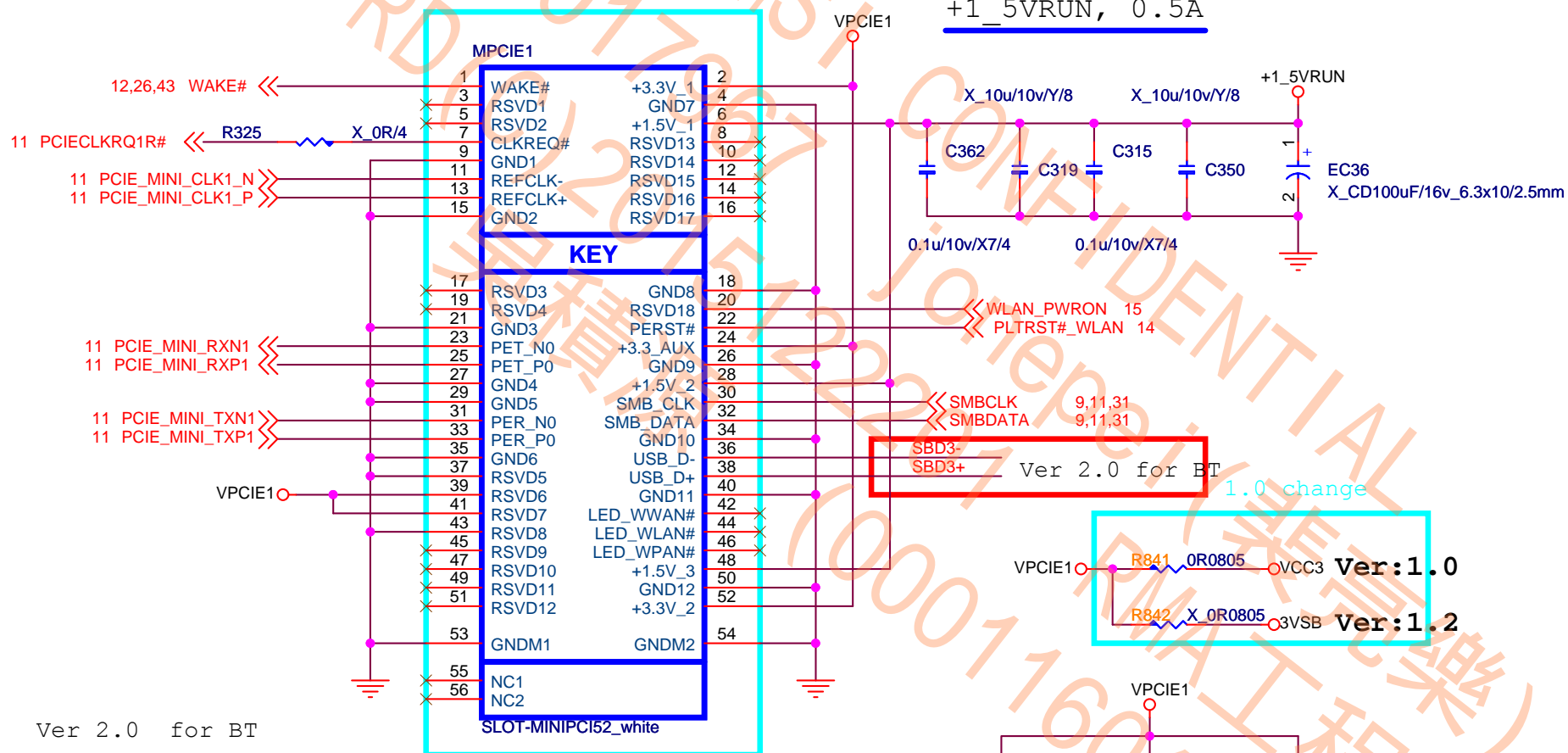


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Wireless Card

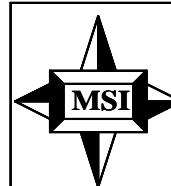
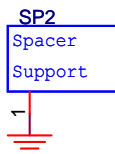
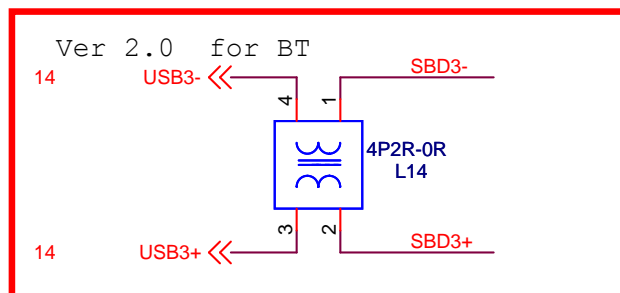
VCC3, 1.5A

+1 5VRUN, 0.5A



Ver 2.0 for BT

change to N11-0520240-K06



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Size	A
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Document Description

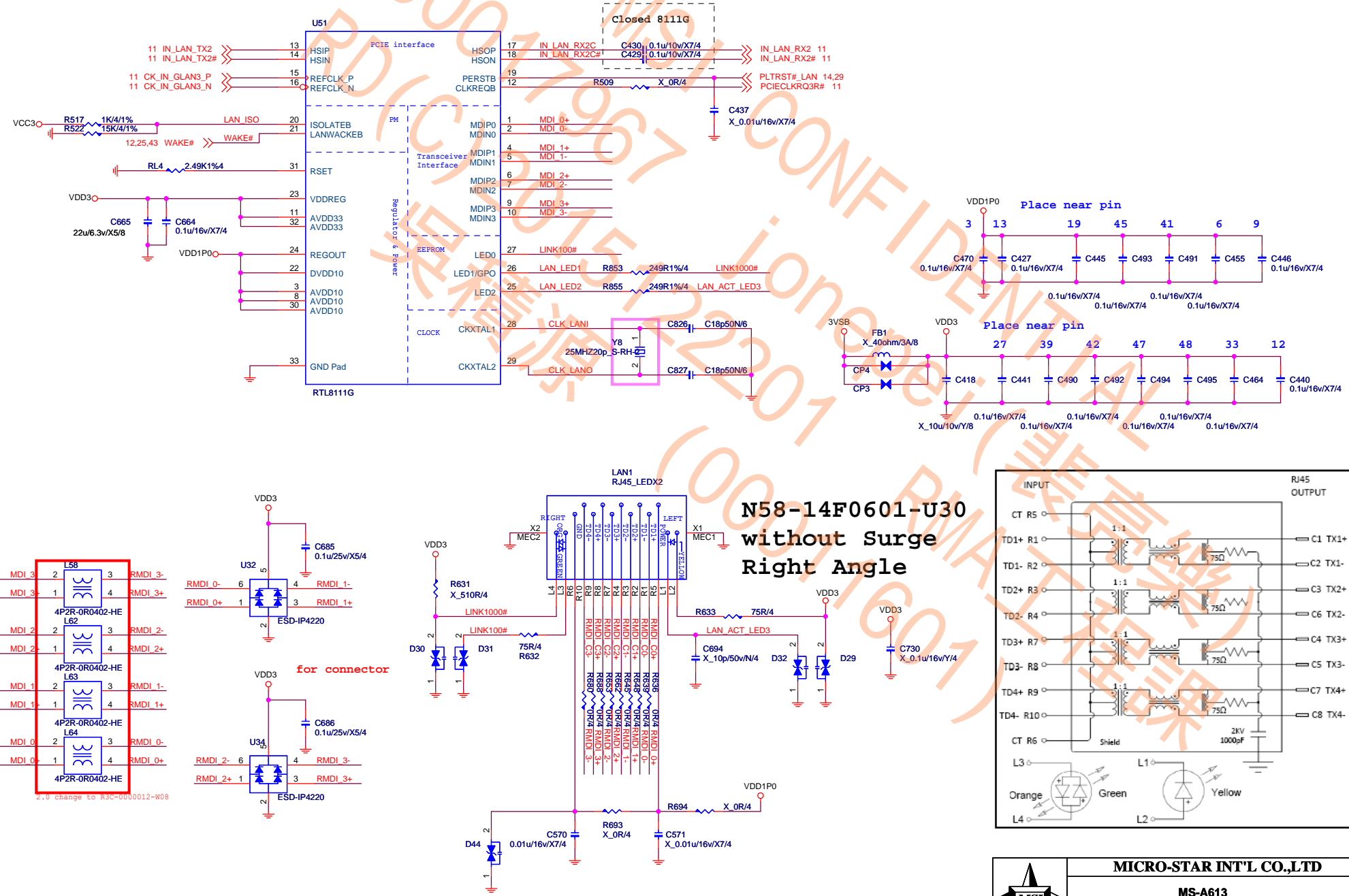
MINI-PCIE Slot

Rev
21


Date: Friday, July 24, 2015

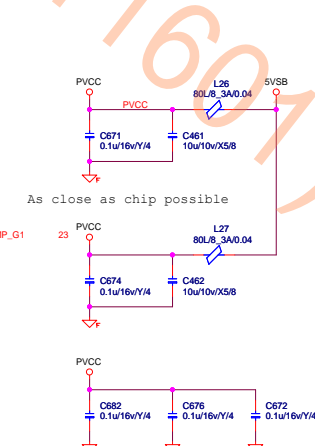
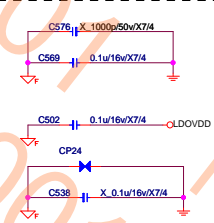
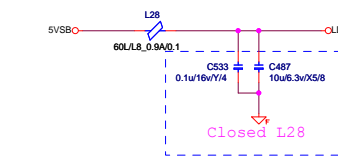
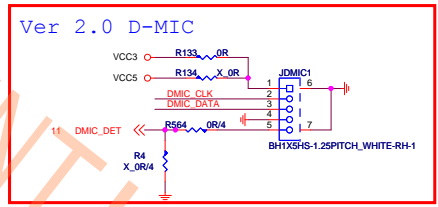
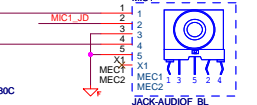
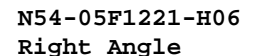
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RTL8111G Giga LAN 1

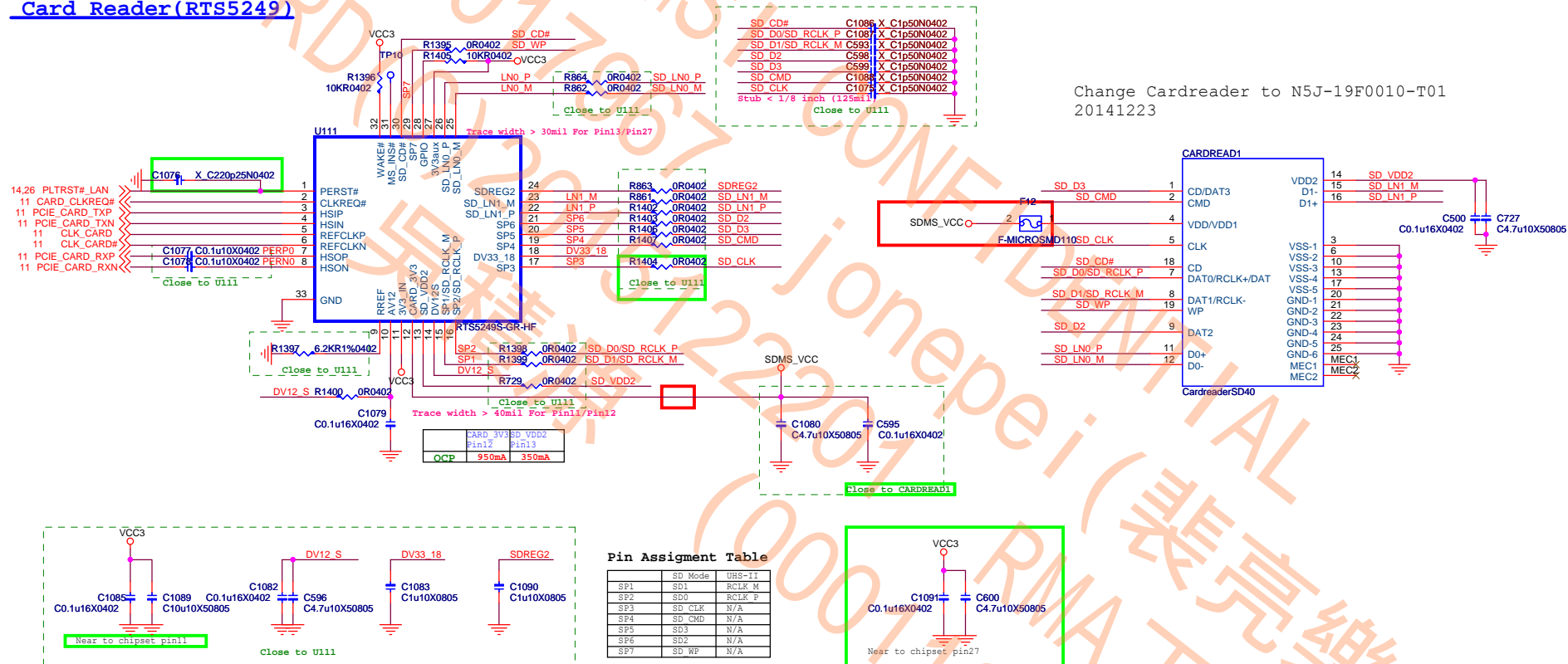


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RD(C)2015122201 RMA工程課
吳積源 (00011601)

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Card Reader(RTS5249)



Pin Assignment Table

	SD Mode	UHS-II
SP1	SD1	RCLK M
SP2	SD0	RCLK P
SP3	SD CLK	N/A
SP4	SD CMD	N/A
SP5	SD3	N/A
SP6	SD2	N/A
SP7	SD WP	N/A

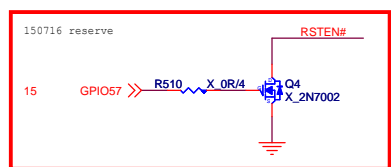
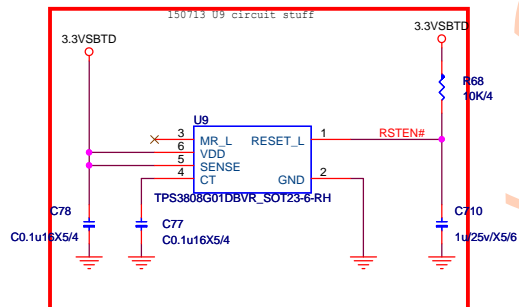
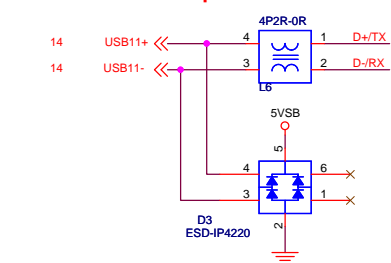


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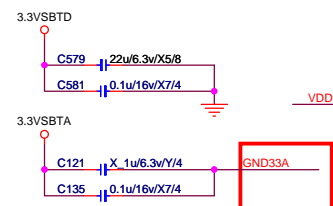
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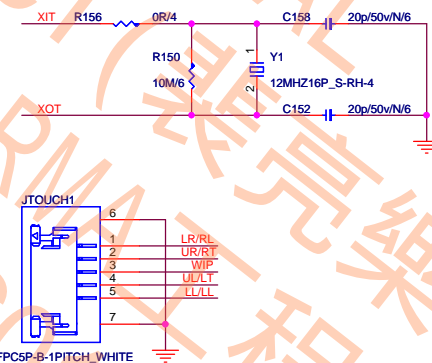
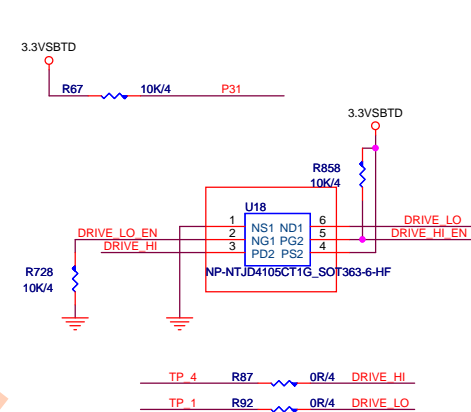
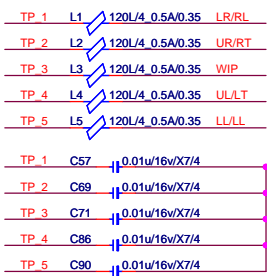
Low Speed USB D+/D-



Decoupling Cap.



EMI Suppressor



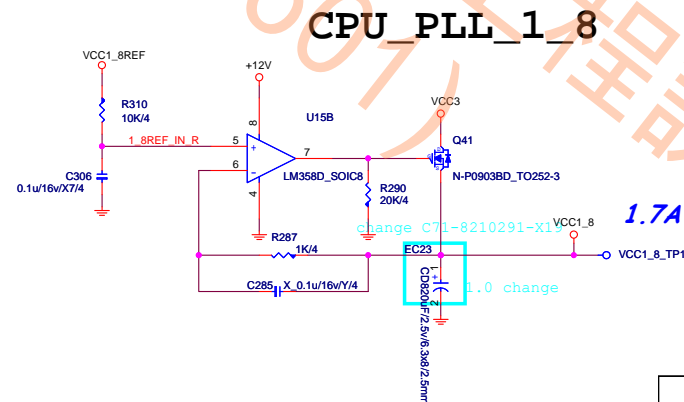
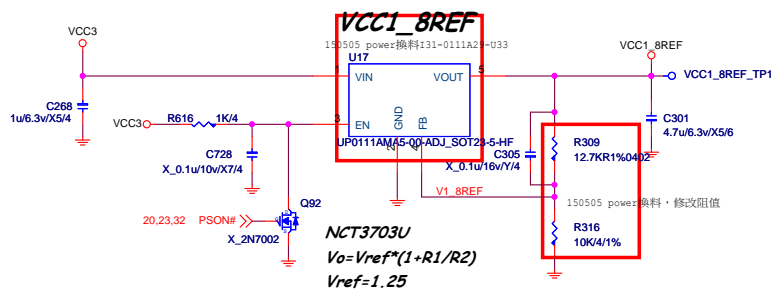
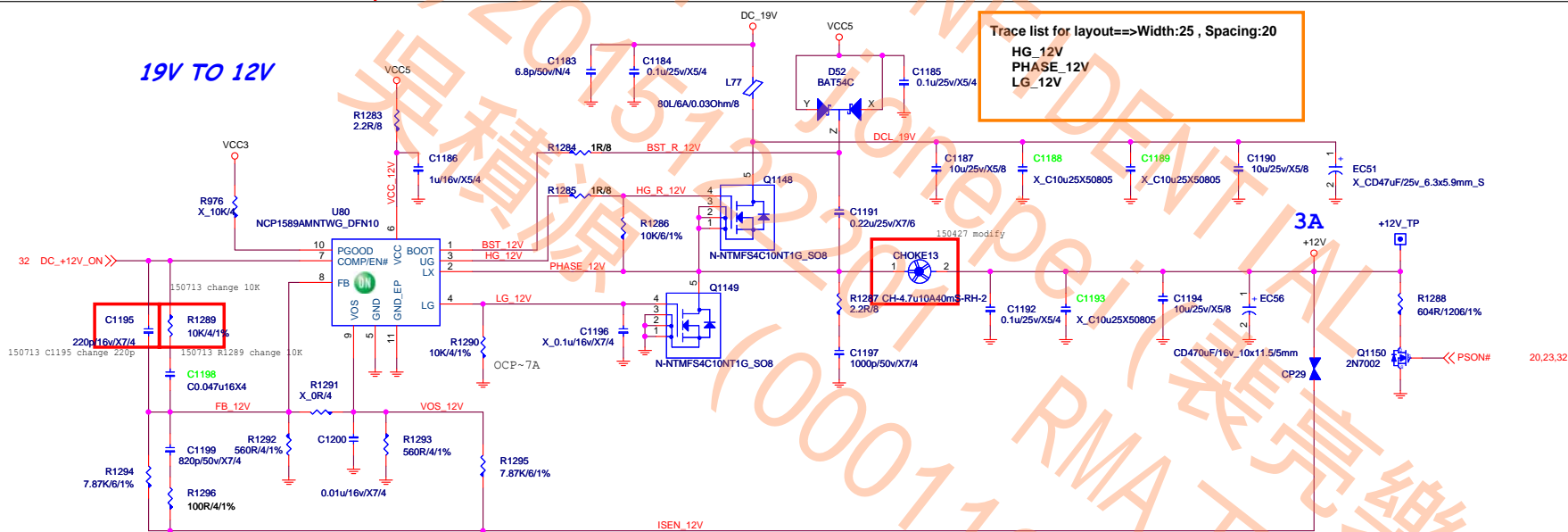
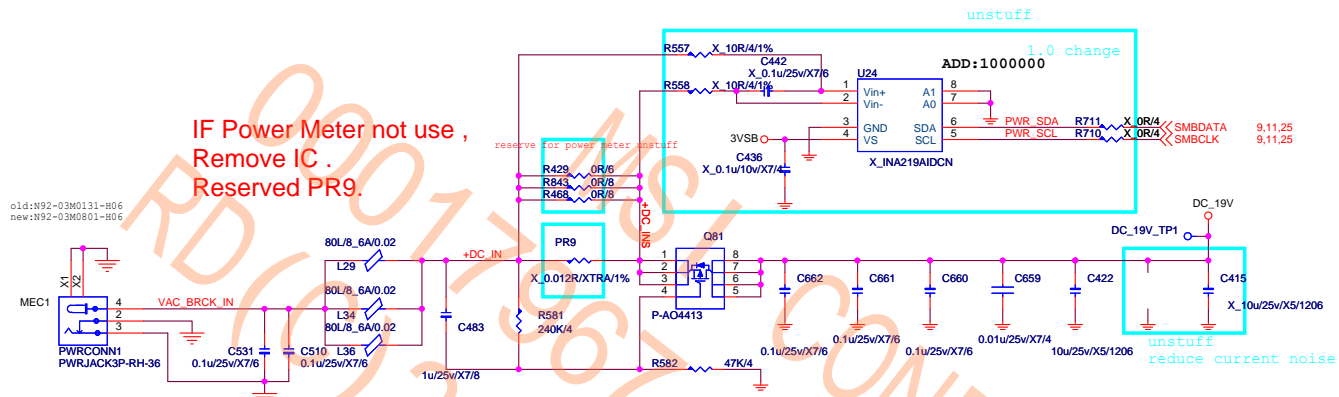
N5A-05F0040-H06
Pitch 1.0mm for 15.6"

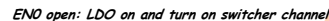
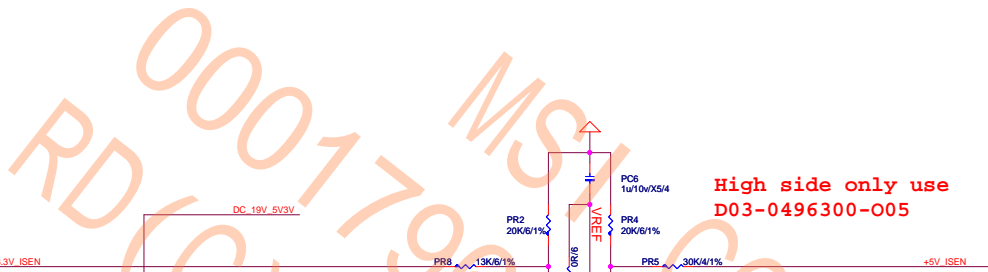



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DDR 3 / DDR 3L VCC_DDR / VTT

VCC_DDR

Current Max at 20A
 DDR_VTT: 1.2A
 +1.5VRUN: 6A
 DDR3 x1 : 4A
 PCH_1P05: 8.16A

VCC_DDR

Current Max at 20A
 DDR_VTT: 1.2A
 +1.5VRUN: 6A
 DDR3 x1 : 4A
 PCH_1P05: 8.16A

TI/TPS51216RUKR I32-512160C-T07

TPS51216

SLUSAB9A – NOVEMBER 2010 – REVISED APRIL 2013

Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

IVB ==> CPU_VTT_SEL : LOW = 1.35 V

SNB ==> CPU_VTT_SEL : HIGH = 1.5 V

6A



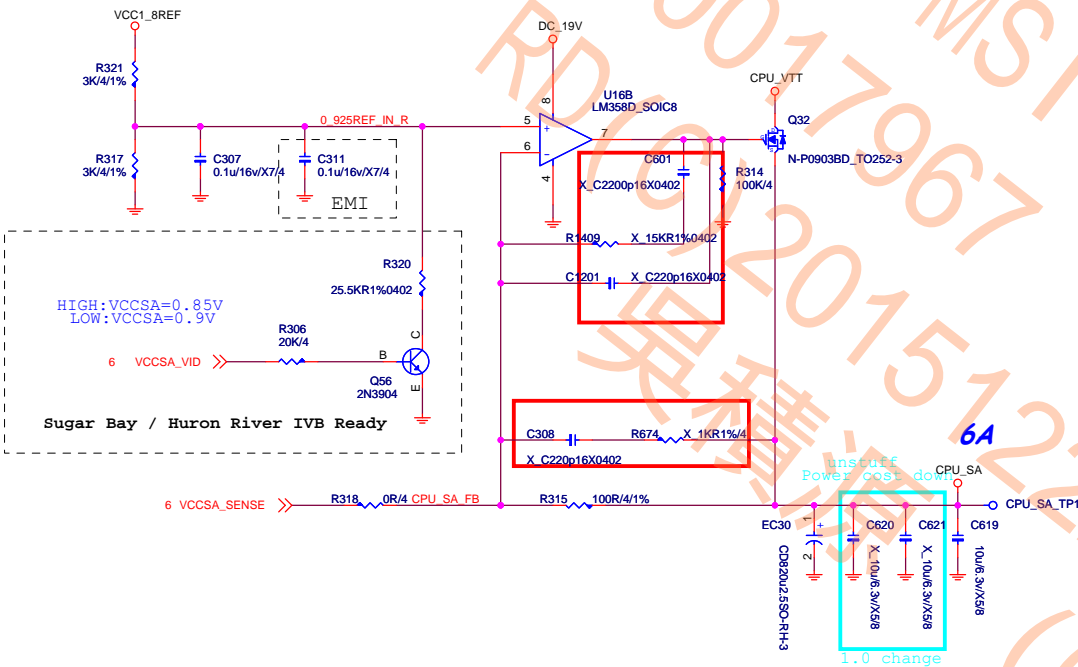
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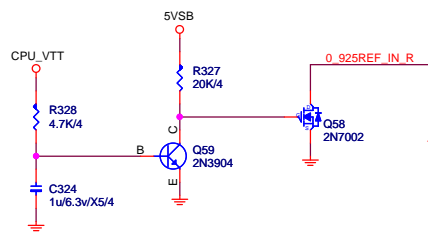
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CPU_SA Power

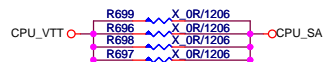
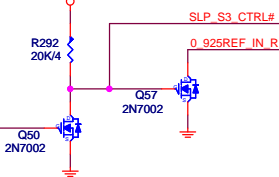
VTT-->CPU_SA



Waitting CPU_VTT Ready

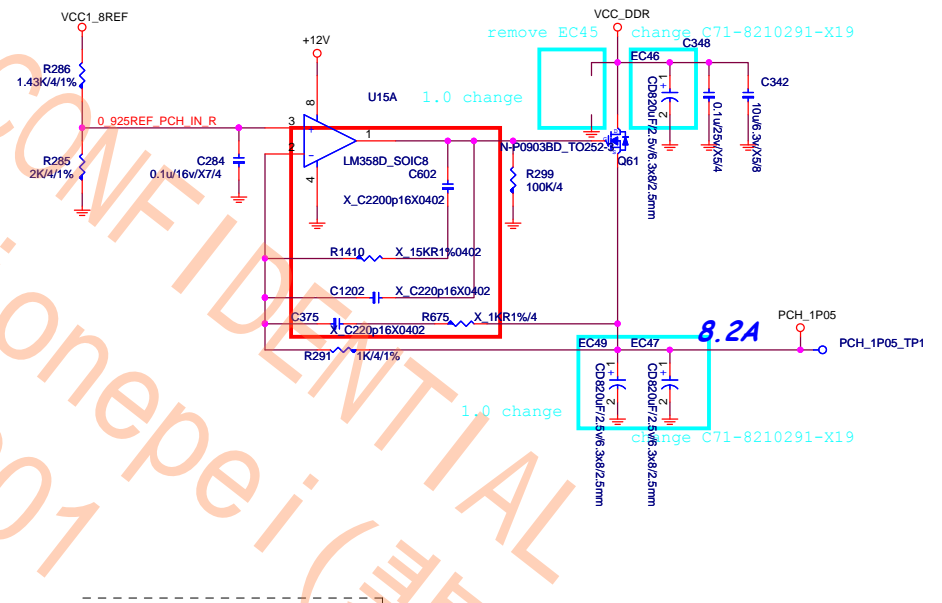


CRB

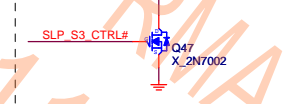


CP Power

DDR-->PCH



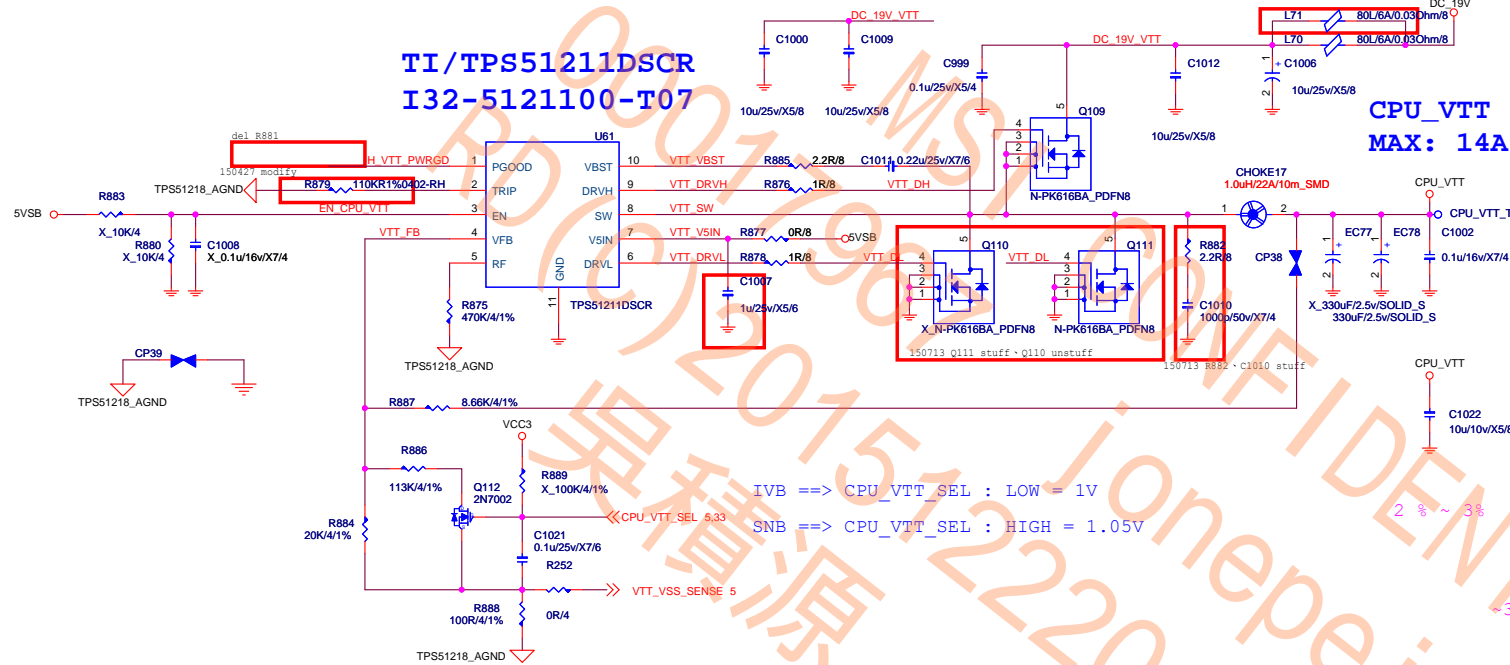
CRB



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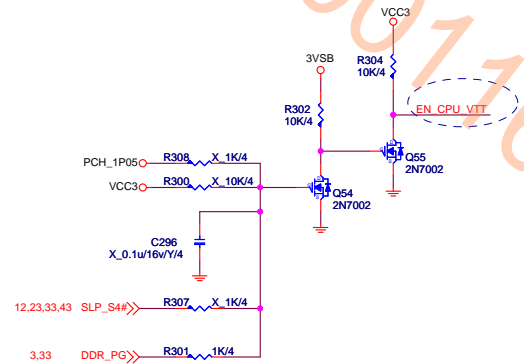
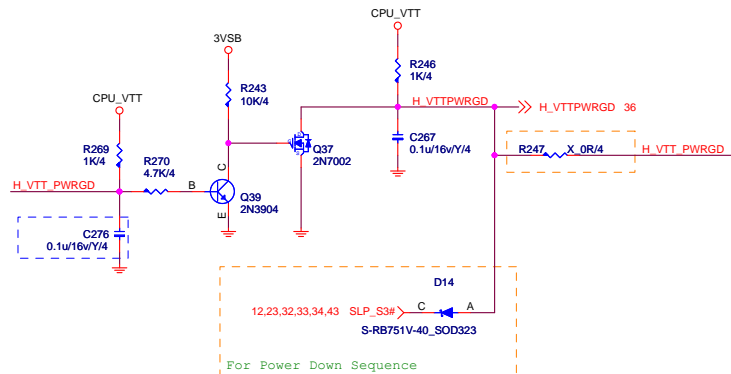
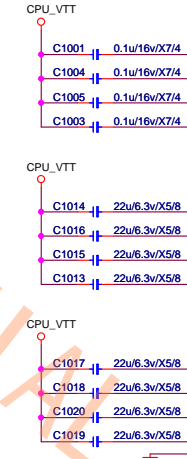


CPU_SA : 6A

CPU_VTT

Current Max at 15A
VCCIO: 8.5A
CPU_SA : 6A

Vo = 1.05
Vin = 19
FS = 300K
OCP 10~14A
Iout = 5.7A
Vin_IRms = 1.3024A
MLCC ripple current = 6A
LIR = 39%
Cin_CAP = 3.3uF
Cout_CAP = 303uF
Cout_CAP_ESR = 8m

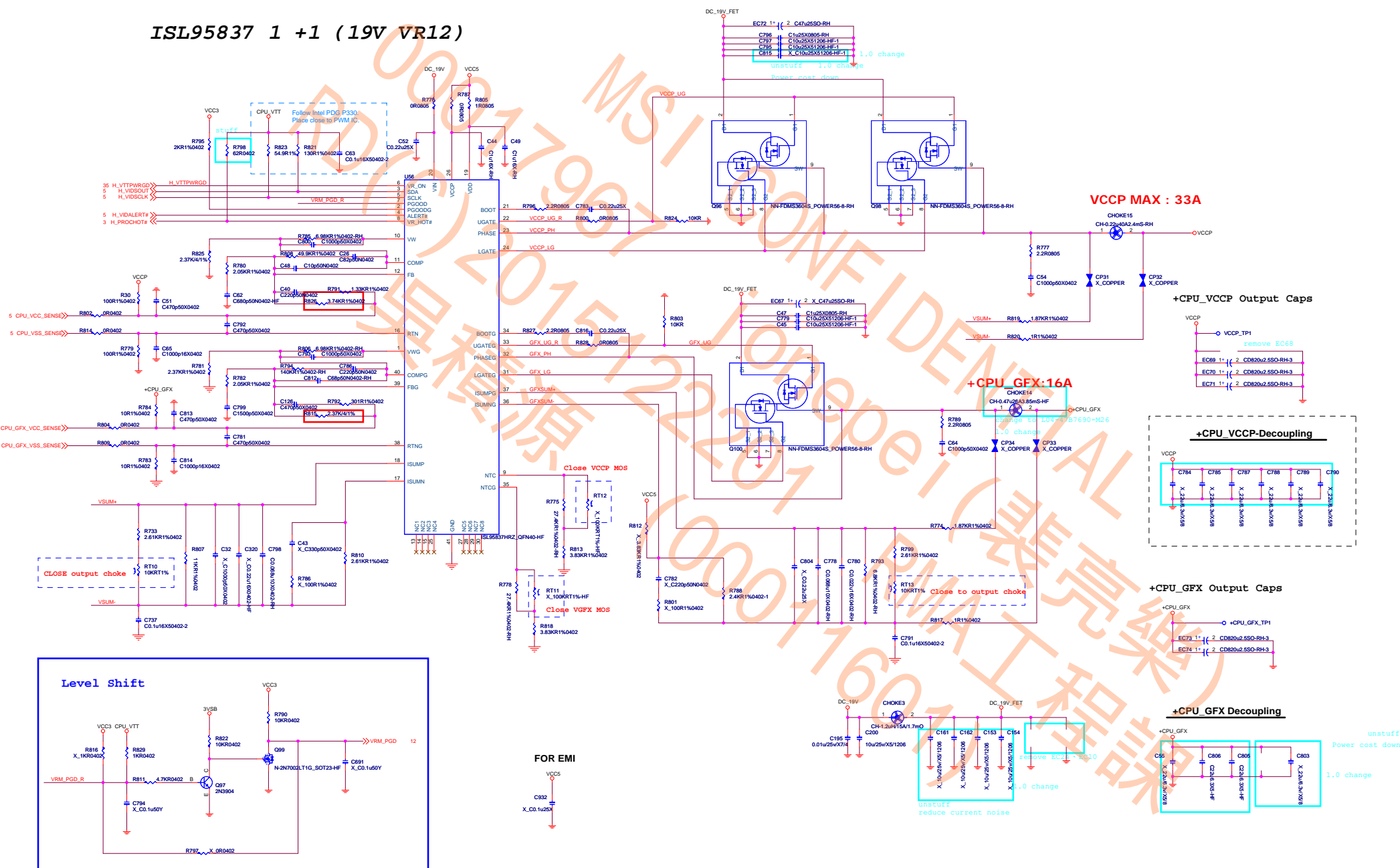


1. Rocset = Iout*DCR/Iocset ; Iocset = 10uA
If DCR = 1m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K
2. Csen = L/Rocset*DCR
If DCR = 1m ; L = 1u, Csen = 1u/2K*1m --> Csen = 0.5U

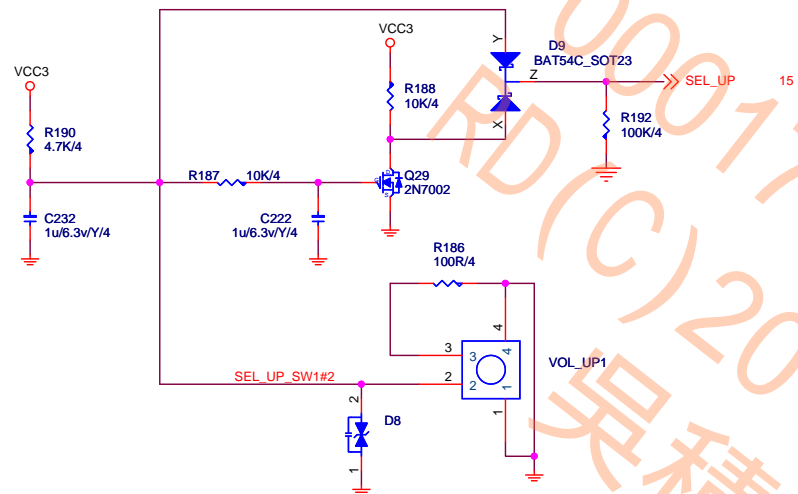


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MS-A613		
Size	Document Description	Rev
Custom	CPU_VTT - TPS51211	21
Date: Friday, July 24, 2015 (Sheet 35 of 43)		

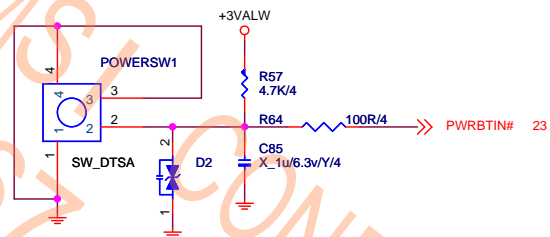
ISL95837 1 +1 (19V VR12)



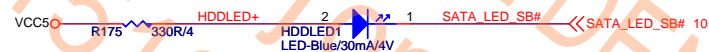
MODE SELECT CONTROL



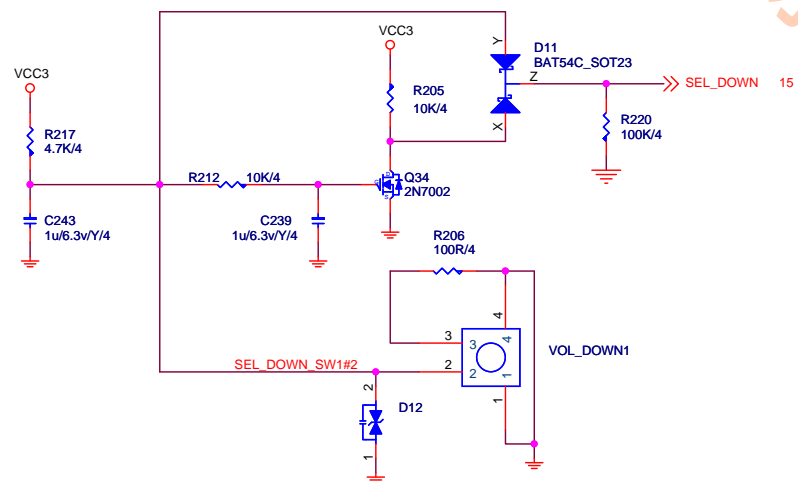
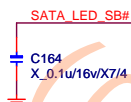
POWER ON/OFF BUTTON



LED Blue

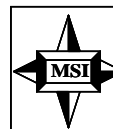
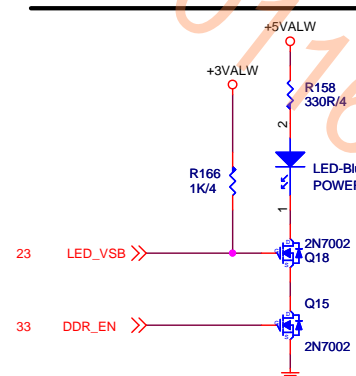


FOR EMI



Ver : 2.0

LED



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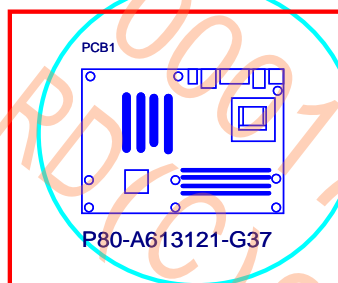
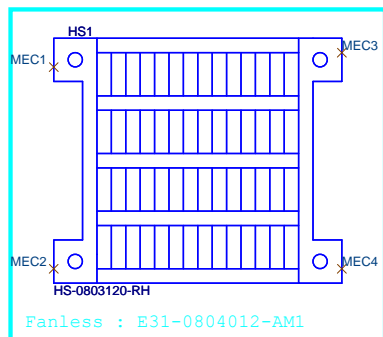
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Size	Document Description	Rev
Custom	HOT KEY / LED	21

Date: Friday, July 24, 2015

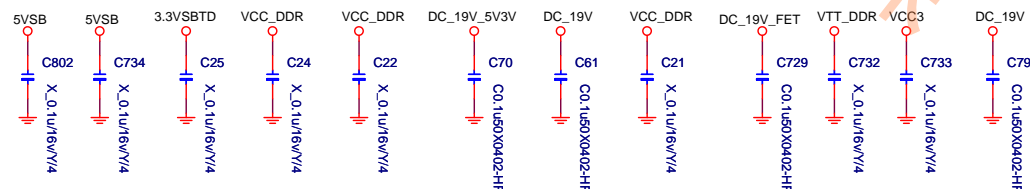
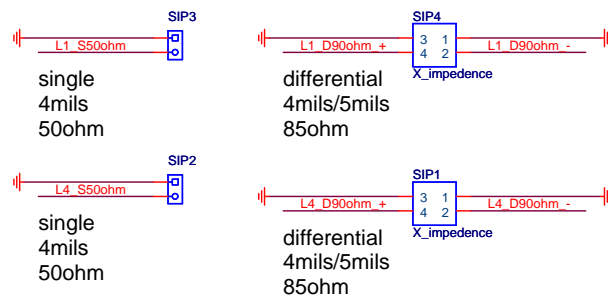
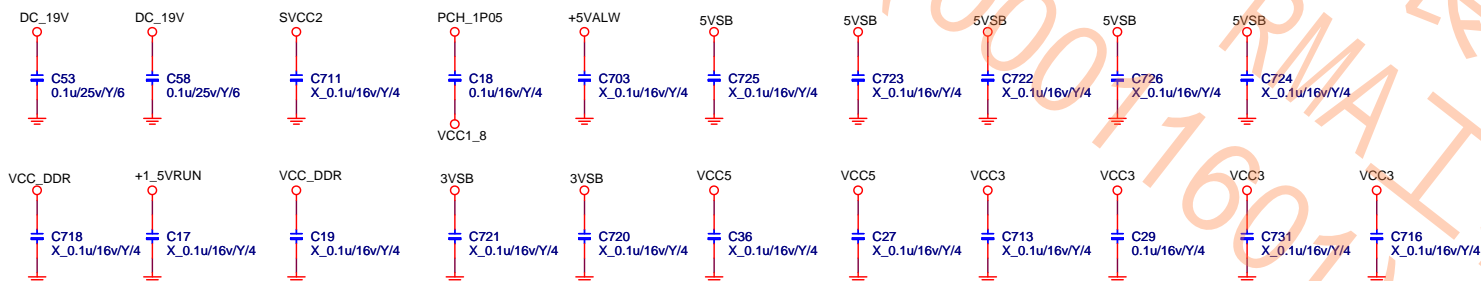
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E31-0406280-AM1



150716 del DHS1

The diagram shows three test points labeled T1, T2, and T5. Each test point has a blue square component with a cross-hatch pattern, representing a test probe or component. Below each component is a red ground symbol. The components are labeled with the text 'X_E23-5566060' above them.



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Manual parts

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LGA988- CPU (35W)	
CPU CORE	- 53A
+1_5VRUN	- 5A
CPU_SA	- 6A
VCC1_8	- 1.5A
CPU_VTT	- 8.5A
CPU_GFX	- 33A

PCH	
CPU_VTT	- 0.6A
VCC1_8	- 0.2A
PCH_1P05	- 8.16A
VCC3	- 0.7A
3VSB	- 0.2A
VCC5	- 0.01A
5VSB	- 0.01A
VBAT	- 6uA

REALTEK/RTL811E-VB	
3VSB -> VDD3	0.17A

HD Audio ALC887	
VCC3	- 0.012A
5VSB -> LDOVDD	- 0.05A

AMP TPA2008	
VCC5 -> PVCC	- 1.5A

DDRIII x2 & TERMINATOR	
VTT_DDR	- 1.2A
VCC_DDR	-8A

SATA HDD /SATA ODD	
VCC5	-3A

(LVDS) LCD PANEL	
VCC5 -> LCD_VDD	- 1.5A
(IRUSH)	-3A

USB 2.0 PORT X4	
5VSB -> SVCC1	- 4A
5VSB -> SVCC2	- 4A

USB 3.0 PORT X2	
5VSB -> SVCC4	- 3A
5VSB -> SVCC5	- 3A

NCP6151/6131	
CPU CORE	0.3V~1.35V - 53A
+CPU_GFX	0.0V~1.3V 33A

NCP5217AMNTXG_QFN14	
VCC_DDR	1.5V 24A

NTMFS4841NHT1G_SO8	
VCC1_8	1.8V 1.7A

NTMFS4841NHT1G_SO8	
CPU_SA	0.925V 6A

NTD4809NT4G_DPAK3	
PCH_1P05	1.05V - 8.16A

NCP5217AMNTXG_QFN14	
CPU_VTT	1.05V 24A

W83310DG_SOP8	
VTT_DDR	0.75V - 1.2A

N-AO4468_SOIC8	
+1_5VRUN	1.5V - 6A

Mini PCI-E slot x2	
VCC3	- 2.75A
3VSB	- 2.75A
1.5V -> +1_5VRUN	- 1A

BlueTooth	- 0.5A
-----------	--------

Level Shifter	- 0.15A
---------------	---------

Webcam	- 0.5A
--------	--------

Card Reader	- 0.3A
-------------	--------

ASMedia USB3.0	
ASM_1P2	- 0.75A
ASM_1P2_SB	- 0.2A
VCC3	- 0.75A
3VSB	- 0.2A

+12V CPU & SYS FAN	- 1A
--------------------	------

INVERTER	- 1A
----------	------

VCC5	VCC3
7.5A	7.626A+EDP_VDD

5VSB	3VSB
14.5A	8.036A
+5VALW	+3VALW
0.5A	0.5A

TI/TPS51120

+12V	
NCP1587DR2G_SOIC8	

+19V	
ADAPTER	



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	Power Delivery	
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SYS5VSB_OFF

SYS5VSB_OFF

TPS51125

VCCRRTC (MB-->PCH)

RTCRST# (MB-->PCH)

5VSB

3VSB

RSMRST# (By SIO to PCH) (SIO delay 66ms as VSB arrives at 2.95V)
up: 2.95V down:2.35VDPWROK (By RSMRST# to PCH) (SIO delay 66ms as VSB arrives at 2.95V)
up: 2.95V down:2.35V

PWRBTIN# (to SIO to PCH) (CP Internal 16ms debounce)

S5# (By PCH to SIO)

S4# (By PCH to ???)

S3# (By PCH to SIO)

PSON# (By SIO to PS)

12V (By PS to MB)

5V (By PS to MB)

3V (By PS to MB)

NCP5217 VCC_DDR (By SLP_S4#/19V)

W83312SN VTT_DDR (By VCC_DDR)

OP+MOS VCC1_8 (By +12V & 3.3V)

OP+MOS PCH_1P05 (By VCC_DDR)

NCP5217 CPU_VTT (By PCH_1P05/19V)

VCCSA_VID (By CPU_VTT)

OP+MOS VCC_SA (By CPU_VTT)

VR_EN (By CPU_SA & +12VIN)

ATX_POK (By PS to SIO 12V/5V/3V Delay 100ms-500ms)

CHIP PGD (By ATX_POK & 3V & S3#) (SIO to PCH) (delay 400ms)

MEM_PWRGD (By PCH to CPU) (as CHIP PGD)

PCH_CLK (By PCH to CPU) (as mem PGD)

CPUPWROK (PCH to CPU) CPU: 5ms min*2, 650ms max

SVID (By VR_EN Ready (>Vih)) (5ms max, VR_EN)

NCP6151 VCCP

VIDALERT# (By VCCP Ready)

VRM_PGD (VR12 to CLK & PCH) (By VIDALERT Ready)

PLTRST# (PCH to CPU) (By PCH to CPU/SIO) (2-21-->2-22 delay > 1ms)

CPURST# (PCH to CPU) (By PLTRST#) (2-22-->2-23 delay > 1ms)

NCP6151 +CPU_GFX

5VSB

3VSB

RSMRST#

PCH_1P05 (as +12V)

CPU_VTT (as +12V)

VCC1_8 (as +12V & 3V)

VTT_DDR

VCC_DDR (as S4#)

12V/5V/3V (as ATX_POK)

ATX_POK (as PSON#)

PSON#

S5#

MEM_PWRGD (as S4#) (must fall before S4# or within 100ns)

S4# S3-->S4-->S5: min 30us

VR_EN (as CPU_SA) T: ????

VCC_SA (as S3#)S3-->S4-->S5: min 30us

CHIP PGD (as S3#)

S3#

VRM_PGD (as VCCP)

VCCP (as VIDALERT#)

+CPU_GFX (as VIDALERT#)

VIDALERT# (as SVID)

SVID (as CPUPWROK)

PCH_CLK

CPUPWROK (PLTRST#-->CPUPWOK >30us)

PLTRST#

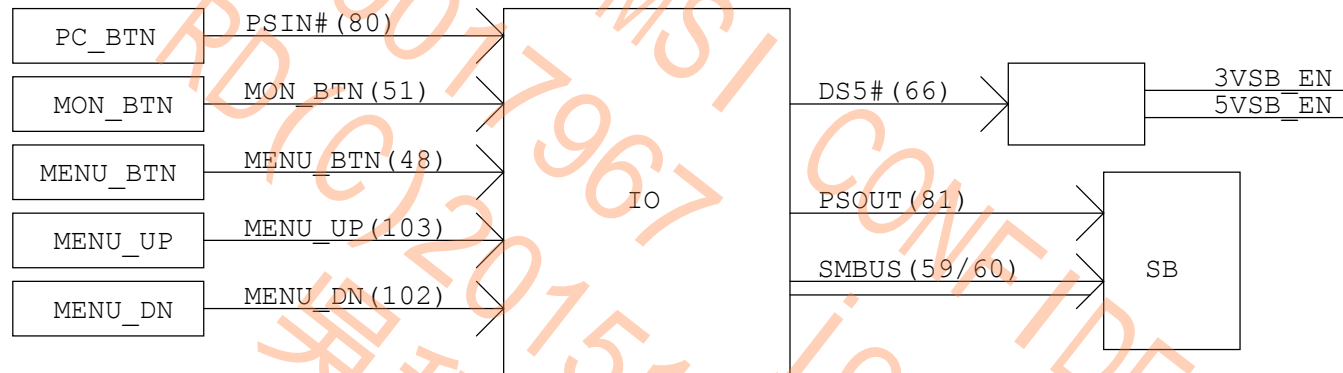
CPURST#



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A613(A615) Schematic History(2.0)

2015/03/26 2.0 circuit(change from A613 1.0)
LVDS線路改EDP線路
SIO(U59)改NCT6104
COM port 2個改4個
Lan connector 2個改1個 , chip 換PTL8111G
AMIC線路改DMIC線路
Card reader改SD 4.0[chip(U111)換RT5249]
U58改MER4485(single touch)
Asmedia USB3.0(U57)換ASM1042AE
DDR power(U60)換TPS51216
CPU VTT power(U61)換TPS51211

PCB 2.1 Hostory

2015/07/14
Page.33 U60 pin.17 , add R881 , C712 , R148(reserve) .
2015/07/20
Page.36 CP31 , CP32 , CP33 , CP34 footprint change NC_93519_2
2015/07/22
Page.22 L51 , L54 , L59 , L61 change L12-9008080-P01
Page.X Add C657 , C667 , C668 for EMI

2015/07/13
Page.38 del HS1 , DHS1 change E31-0804012-AM1
Page.33 Q108 , R847 unstuff
R868 change 12.1K
Page.23 R973 , R1009 unstuff , R60 stuff
Page.20 R210 unstuff , R209 stuff
Page.30 U9 circuit stuff
Page.36 power team suggestion:
R826 change 3.74K , R815 change 2.37K
Page.33 R870 , C944 stuff
Page.35 Q110 unstuff , Q111 stuff
R882 , C1010 stuff
Page.31 R1289 change 10K , C1195 change 220p
Page.28 JAMIC1 unsuff
Page.23 R991 unstuff,R993 stuff

